Analytical Modeling of Silicon Nanowire Transistor - Effect of Width Variation

By

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Abstract

The effect of width variation of a Silicon nanowire MOSFET is studied in this work. We considered a ballistic gate-all-around Silicon nanowire MOSFET. The eigen energies of the time independent Schrodinger's equation were found by solving the Bessel's function. The eigen energies were used to find the drain current. We have used an analytical compact model to calculate the drain current. The effect of width variation on the drain current, transfer characteristics, transconductance, subthreshold swing, saturation current and saturation current density of the device are investigated.

According to our observation the subthreshold swing decreases and the peak of transconductance increases as the wire widens. Saturation current increases with increase in width. Increase in saturation current density with decrease in wire width is an important motivation for choosing narrow wires in MOSFETs.

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We are sincerely grateful to Professor Anisul Haque, Department of Electrical and Electronic Engineering (EEE), East West University (EWU), Dhaka, our supervisor, for his patience, support, supervision and valuable suggestions throughout our work.

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EWU, Dhaka Authors

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Approval

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Authorization page

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Rokhsana Ahmed

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Chapter 1 : Introduction

1.1 Background

MOSFET (Metal Oxide Semiconductor Field Effect Transistor) was first proposed by Julius Edgar Lilienfield in 1930 [1]. The first MOSFET was fabricated in 1960 and it took 30 years to overcome the effect of surface states at the interface between the oxide and the semiconductor of the device. Today Silicon MOSFET is the workhorse of the IC industry.

To fit the IC scaling trend, the transistors had to be periodically shrinked from all directions. The prediction about scaling of transistors was done by G. E. Moore and is known as the Moore's law [2].

As the devices became smaller, it produced some unwanted effects, for example, the Short Channel Effect (SCE) becomes severe and it becomes difficult to turn off the device. Drain Induced Barrier Lowering (DIBL), mobility degradation, sub-threshold conduction and velocity saturation are few other problems. Different types of devices are considered to overcome these limitations. When the downsizing of the devices reached the atomic limits, the device architectures went through changes to increase the gate control of the channel and to meet the requirement of the designers. The state-of-the-art transistors include Silicon-on-insulator (SOI) MOSFETs, finFETs and Silicon Nanowire (SiNW) MOSFETs. The channel of a SOI MOSFET is isolated from the semiconductor substrate by a buried oxide layer. The conducting channel of a finFET consists of a thin Silicon fin which forms the body of the device. The channel of a SiNW MOSFET is made of a narrow Silicon wire which joins the source and drain. The wire is wrapped by the gate so the control of the gate is improved.

1.2 Literature Review

SiNW MOSFETs became popular because of its ability to suppress SCE and thus lowering the off leakage current [3]. It is compatible with the existing CMOS technology [4]. The nanowire transistor is different from a conventional one because the scattering effect is very significant in a conventional MOSFET. For a nanowire MOSFET, the mean-free-path is comparable to the dimension of the device and so the scattering effect and carrier mobility is ignored [5]. As the wire thins, the confinement energy of the carriers increase reducing the barrier height from the

subband bottom. This results in an increased threshold voltage so turning on the device becomes difficult.

The research on nanowires speeded up in 1998 when SiNWs with diameters less than 20nm and lengths greater than 1μm were demonstrated using laser-ablation method [6]-[7]. Many attempts have been made to fabricate SiNW transistor using both back gate [8]-[9] and gate-all-around (GAA) geometries [10]-[13]. Successful fabrication of transistors was done using NWs as building blocks [14]. The group of Lieber reported controlled doping of SiNW devices [15] along with diameter controlled synthesis of NWs [16]-[17], multishell Si-Ge nanowire heterostructures [18] etc.

Some important theoretical analyses were done by Cui et al in 2002. They tested the effect of source-drain contact thermal annealing and surface passivation on key transistor properties. The average transconductance and average mobility were found to increase to very large values [19]. Lieber and others presented the advantages of heterostructure NWs as compared to homogeneous NW devices. They also discussed basic methods of organizing NWs to be used in fabrication. They introduced the concept of crossbar NW circuits and the application of thin-film transistor array [20].

In 2008 Appenzeller and others discussed the electronic properties of four different NW-FETs, Schottky-barrier NW-FETs with metallic source-drain contacts, conventional NW-FETs with doped NW segment as source and drain electrodes, NW impact ionization FET and Tunnel NW FETs. They used analytical results and experimental data to explain the features of these devices [21]. Later in 2012, Doria and his group proposed a drain current model for triple gate n-type junctionless NW transistors based on the solution of Poisson equation. They used the 2-D Poisson equation to get the surface potential for long channel devices and then the solution of 3-D Laplace equation is added to consider the short-channel effects [22].

To simulate a transistor performance accurately for circuit simulation, it is important to model it properly. The compact model is very useful in this regard. It includes a set of equations whose solution gives the device characteristics. Establishment of the compact model is essential for designers but there are challenges as well. For example I_D-V_D characteristic depends on the band

structure which is very sensitive to the wire width, cross-sectional shape, crystal orientation, mechanical stress etc [23].

Natori showed the physics behind ballistic NW MOSFET. He used a compact model to analyze the I_D-V_D characteristics, sub-threshold characteristics, short channel effects and effects of quantum capacitance on device characteristics. He included temperature effects and relation to quantum conductance [24].

1.3 Objective

The objective of this thesis is to apply an analytical model of a nanowire to find the dependence of a few important parameters on the wire width of a SINW MOSFET. The comparisons for current-voltage characteristics, transfer characteristics, sub-threshold swing, saturation current, saturation current density and transconductance are found for different radii of the nanowire. We analyze the relation between these parameters and the width of the nanowire.

1.4 Thesis Organization

At first we begin with an understanding of the device structure and the operation of a conventional MOSFET. Then the channel formation of a MOSFET is explained. Moore's Law and its effects on the device are discussed in the next section. The chapter ends with how the devices changed to overcome some undesired short channel effects and how the SiNW MOSFET evolved.

Next, the introduction of SiNW MOS and its advantages over conventional MOS are given. The model used for analysis is described and the assumptions along with necessary conditions are given. Equations related to the study and all relevant parameters are also presented. Finally, the results of the study are shown using illustrations and tabular formats. The results are compared to show the effect of wire width on the device performance. At last, a conclusion is drawn and further scopes of work are also mentioned.

Chapter 2 : Scaling and Limitations of Conventional MOSFETs

2.1 MOSFET Overview

MOSFETs use the electric field across the oxide to form a conducting channel between the source and drain. A basic illustration of a four terminal n-type MOSFET is shown in figure-2.1. The gate creates a conducting channel between the source and drain. The channel formation is explained in the following section.

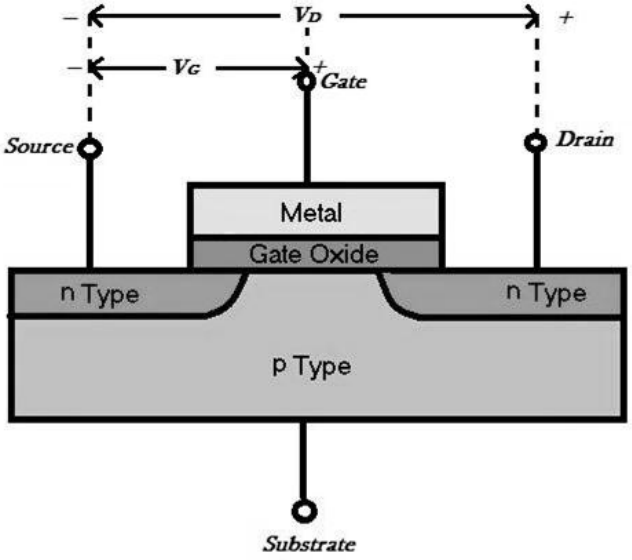

Figure 2.1: The basic structure of a NMOS.

2.1.1 Energy band at inversion

There are four modes of operation of a MOSFET depending upon the gate biasing. The modes of operation are flatband, accumulation, depletion and inversion [25]. The channel formation happens at inversion. If the gate is positively biased and if the biasing is gradually increased, the energy bands will bend and at one point the intrinsic Fermi energy level will cross the Fermi energy. This is shown in figure-2.2. At first the holes are depleted but when the electric field is very strong the minority electrons will feel the force and get attracted to the surface. This phenomenon is called inversion. The signature of inversion is that the semiconductor surface behaves like n-type. If we have a source on the left and drain on the right hand side of the device, the electric field will be towards the left and current will depend on the availability of charge

carriers. Thus a channel is formed between the source and drain. The general equation of the drain current is shown in equation (1).

$$I_D=\left(\frac{W}{L}\right)\mu_n C_{ox}\left[(V_G - V_T)V_D - \left(\frac{{V_D}^2}{2}\right)\right] \ldots\ldots\ldots (1)$$

Where, W= gate width, L= gate length, μ_n=mobility, C_{ox}= oxide capacitance, V_T = threshold voltage, V_G= voltage drop across gate and source and V_D= voltage drop across drain and source.

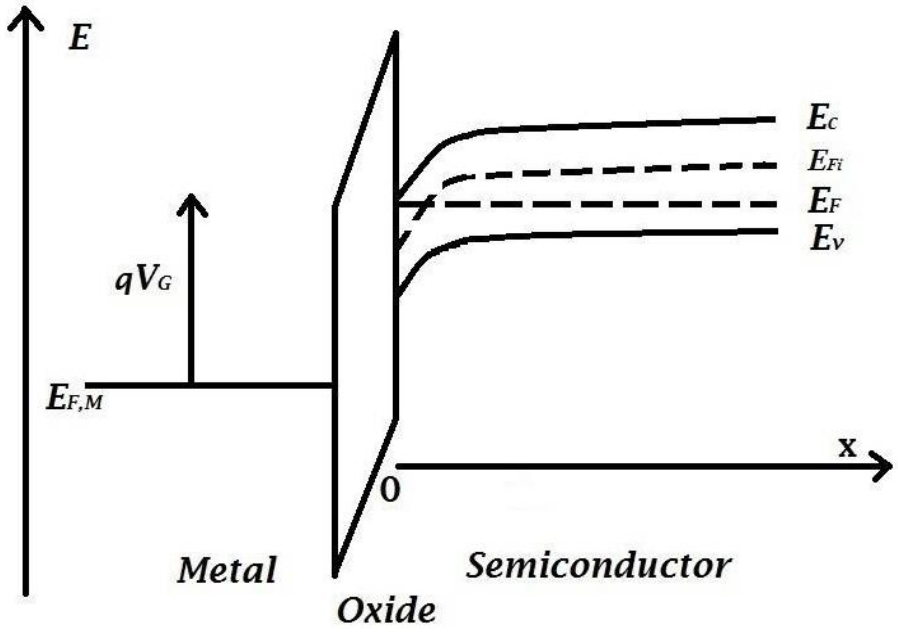

Figure 2.2: Energy band diagram of NMOS at inversion.

2.2 Transformation of MOSFET with time

MOSFET ICs are used in most of the electronic devices and few important factors have to be considered to meet the demands of the trend. They are cost, speed, power consumption and area. The area is one factor that has undergone huge changes because electronic devices have only got smaller from time to time. This miniaturization of transistors is known as scaling. In this regard Gordon E Moore made a very important observation which is discussed in the following sub-section.

2.2.1 Moore's Law

In 1965 Gordon E Moore (founder of Intel) said that for minimum cost, the number of components per integrated circuit would be 65,000 by 1975. He believed that it was possible to fit such a circuit on a single wafer [2]. He also said that the number of devices on a chip doubles every 18 months. This is known as Moore's Law and the observations are illustrated in figures 2.3 and 2.4.

After the scaling of the planar MOS reached atomic limit, the geometry of the device had to be changed to improve control over the device. The transformation of the appearance of MOSFET with time is shown in figure-2.5. The single gate SOI (Silicon on Insulator) MOSFET was advantageous because of its ability to suppress the short channel effect, lower parasitic capacitance and a high packing density. After the single gate MOSFET, came the double gate SOI transistor which was introduced by Sekiwaga and Hayashi [26] in 1984. They showed that the short channel effect could be eliminated in this type of structure. The volume inversion layer was located at the centre of the device rather than the Si/SiO_2 interface. In 2003, Lemme et al introduced the Tri-gate MOSFET [27]. The channel is isolated from the substrate by a buried

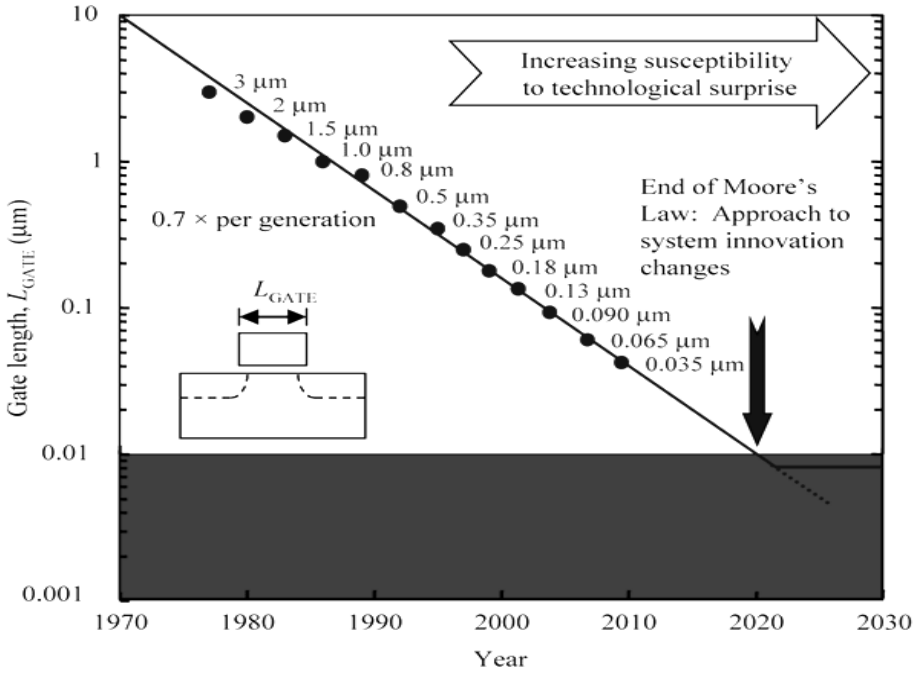

Figure 2.3: Change of channel length of MOSFET with time [28].

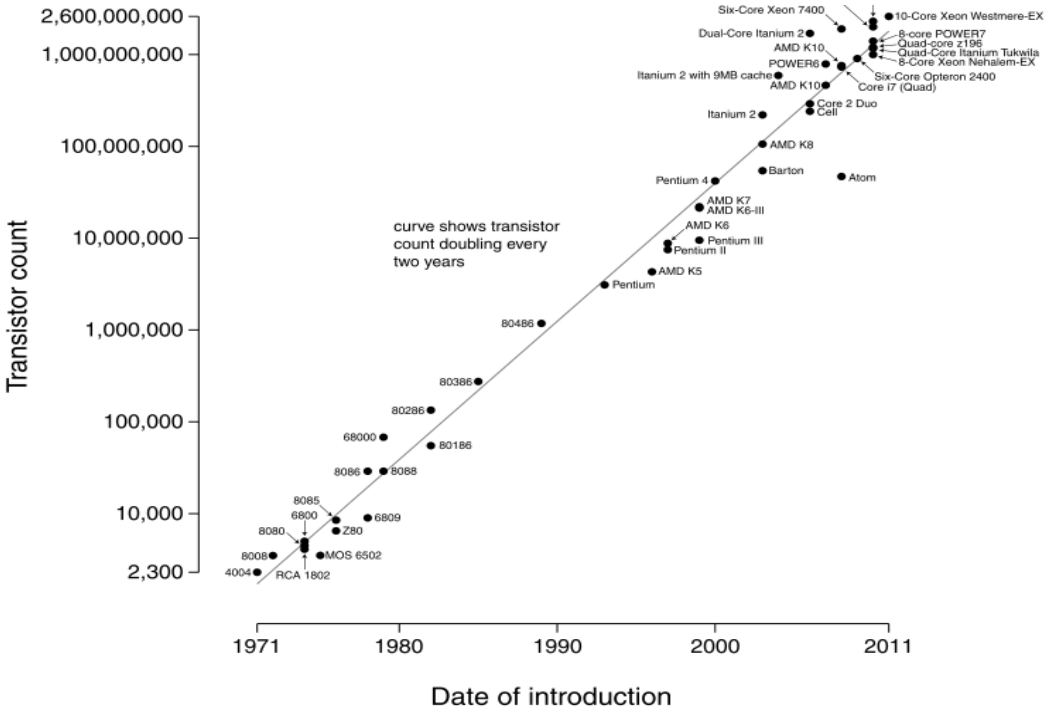

Figure 2.4: Increasing number transistors with each new microprocessor technology [29].

oxide layer which helps to improve the substrate noise and then FINFETs were introduced. FinFETs operate at low voltages and consumes less power. The off current is also small which means the junction leakage is reduced [30]. Later the channel was controlled from all four sides using the quadruple gate or gate-all-around FET. They have high packing density which is good for memory devices and the DIBL is best suppressed by this structure [31].

Finally the research on Nanowire FET is attracting much interest today even though the first publication on Silicon wire growth was by Treuting and Arnold in 1957 [32]. Both quadruple gate FET and SiNW FET are gate-all-around transistors. When the cross-sectional dimensions of the channel of a quadruple gate FET falls in the nanometer regime, it is called a nanowire transistor. The advantages of a SiNW FET will be discussed in the next chapter. It is due to these technological innovations that Moore's law will hold true in future.

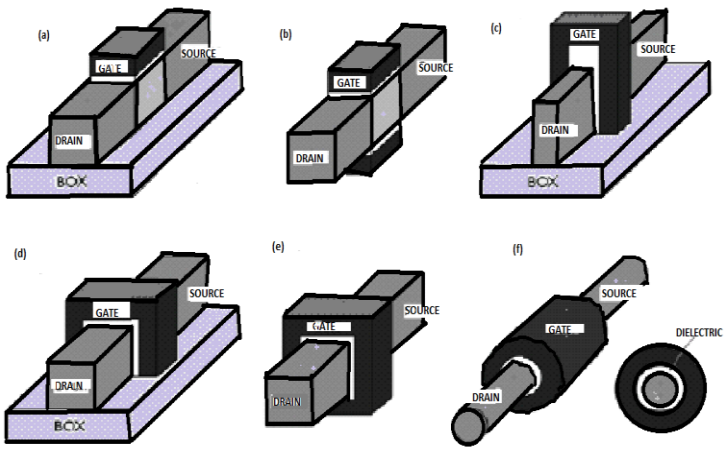

Figure 2.5: (a) Single gate SOI transistor, (b) double gate planar SOI transistor, (c) double gate non-planar FinFET, (d) trigate FET, (e) quadruple-gate (or gate-all-around) FET and (f) gate-all around (or surrounding gate) FET (nanowire FET).

2.3 Non-Ideal Effects

The downsizing of the MOSFETs gives birth to some secondary effects. Some of the effects are sub-threshold conduction, short channel effect, drain induced barrier lowering, ballistic transport etc. However, when the technology nodes fall below 0.5µm, the dominant non-ideal effects are sub-threshold leakage current, reverse biased p-n junction leakage and gate induced drain leakage current [33]-[34]. When the channel length is brought down below 100nm, the gate oxide thickness is reduced to attain high current drive capability and to reduce short channel effects. This produces another effect called gate tunneling current. It is produced by the quantum mechanical wave function of a charged carrier through the gate oxide potential barrier into the gate. It depends on the device structure and bias conditions. For sub-50nm MOSFETS the effect that becomes prominent is the body-to-drain junction tunneling current and this happens due to high doping concentrations [31]. Moreover, if V_{DD} increases and approaches the junction breakdown voltage, avalanche current also appears.

Chapter 3 : Silicon Nanowire MOSFET

After FinFETs, the new phase of CMOS evolution began with NW transistors. In this chapter, different aspects of the gate-all-around Silicon Nanowire (SiNW) MOSFET will be described using the analytical model.

3.1 Structure of SiNW MOS

In a cylindrical SiNW MOS, the source and drain are on the extreme ends of the cylinder and the nanowire channel joins them. The diameter of the channel can be as small as 1nm which is wrapped in a layer of oxide covered by a metal gate. These devices are an efficient replacement for planar MOSFETs [35]. For our work, we have considered an intrinsic nMOS of various wire widths made of Silicon. An illustration of the SiNW MOS is given in figure-3.1.

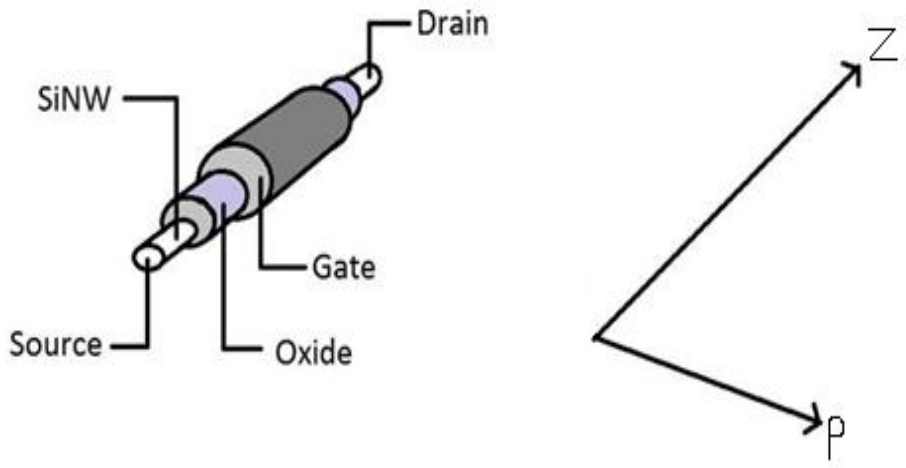

Figure 3.1: Diagram of a next-generation field effect transistor using a silicon nanowire.

A nanowire can be made using both top-down and bottom-up approach. In the top-down technique, a block of the solid material is shaped to form the desired nanowire. The bottom-up approach is like assembling where the core material is added to the wire as it grows and is apparently more advantageous than the other process.

3.2 Advantages of SiNW MOS

Apart from the small diameter, the SiNW has some advantages that make it a preferable choice over other devices. It allows high control over the device current and consumes very small area [24]. The device is compatible with the existing CMOS technology and can be prepared in high-yield and reproducible electronic properties as needed by the large-scale integrated systems [36]-[37]. Since the channel length of SiNW MOS is small, the body of the semiconductor or the diameter of the nanowire prevents the charge carriers from escaping the gate control and produces high drive current [38]-[39]. Introduction of dopants is not necessary while scaling the MOS. The synthesized material is crystalline and has smooth surfaces. It has the ability to produce radial and axial nanowire heterostructures and thus scattering is reduced and carrier mobility is increased [40]-[41]. The SiNW FETs are ultrasensitive and so they have biomedical applications such as SiNW FET sensors [42].

3.3 Mathematical model

Throughout the work, we have assumed that the MOSFET is ballistic and so the mobility concept does not apply. For ballistic devices Newton's second law of motion is applicable. In these cases we consider that carriers come out of the channel without any kind of scattering, travelling a smooth path. The material of the nanowire is intrinsic Silicon. To analyze a SiNW MOS, we need to know the important parameters and their expressions. The equation for electric current of a ballistic SiNW MOS is shown in equation (2) [24].

$$I_D = G_0 \left(\frac{K_B T}{q}\right) \sum_i g_i \ln \left\{ \frac{1 + \exp\left[\frac{(\mu_s - E_{i0})}{K_B T}\right]}{1 + \exp\left[\frac{\mu_D - E_{i0}}{K_B T}\right]} \right\} \ldots\ldots\ldots (2)$$

Where $G_0 = 2q^2/h = 77.8\ \mu S$ (Quantum Conductance), $\left(\frac{k_B T}{q}\right) = 0.026V$ (Thermal Voltage), g_i (i=0, 1,…) is the degeneracy of the i_{th} subband, μ_S and μ_D are the Fermi levels of the source and drain respectively and E_{i0} is the subband energy. The approximate energy profile along the channel in the x-direction is shown in figure-3.2, where Xmax and Xmin are the maximum and minimum potential energy positions respectively. Figure-3.3 shows how the energy levels are related with one another in the nanowire channel and the electrodes. In the diagram, μ_0 is the

subband bottom of the channel (E_{00}), Φ_1 and Φ_4 are the potential barriers from the gate and substrate Fermi level to the conduction band of the insulators, Φ_2 and Φ_3 show the same barrier but from the subband bottom of the nanowire to the conduction band of the insulators, Φ_G and Φ_P are the bias voltages across the gate insulator and the substrate insulator respectively, V_D and V_G are the external biases.

During our analysis, we considered μ_0 to be the reference and from figure-3.3 we found that $\mu_S - \mu_D = qV_D$ and $\mu_S - \mu_0 = qV_G$. As μ_0 is 0, μ_S becomes qV_G [24]. After substitution of these sub-equations in (2) we get equation (3).

$$I_D = G_0 \left(\frac{K_B T}{q}\right) \sum_i g_i \ln \left\{ \frac{1 + \exp\left[\frac{(qV_G - E_{i0})}{K_B T}\right]}{1 + \exp\left[\frac{qV_G - qV_D - E_{i0}}{K_B T}\right]} \right\} \ldots\ldots\ldots (3)$$

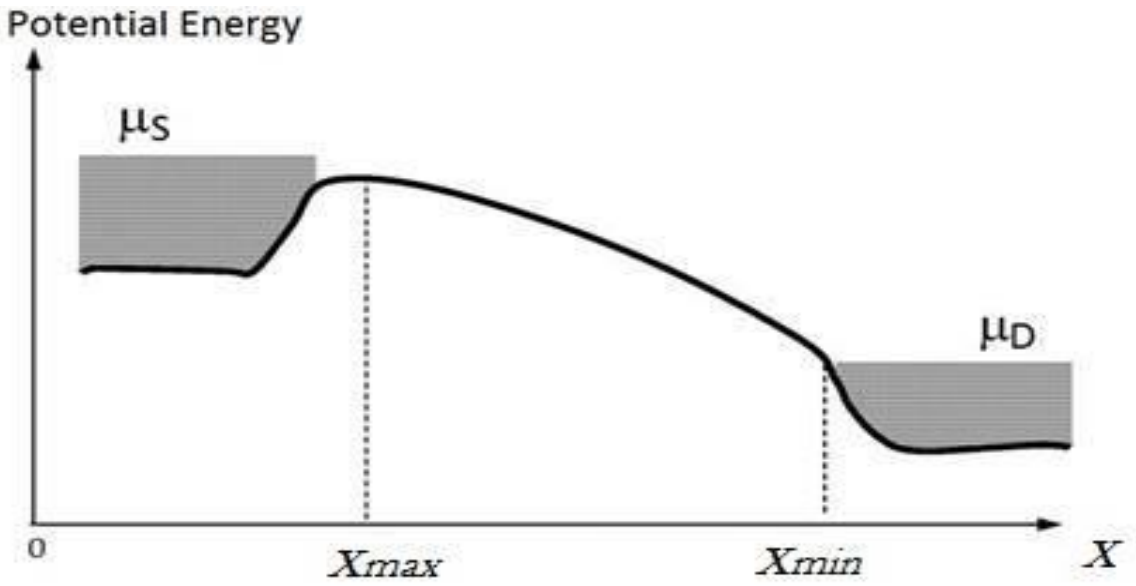

Figure 3.2: Potential energy profile along the channel.

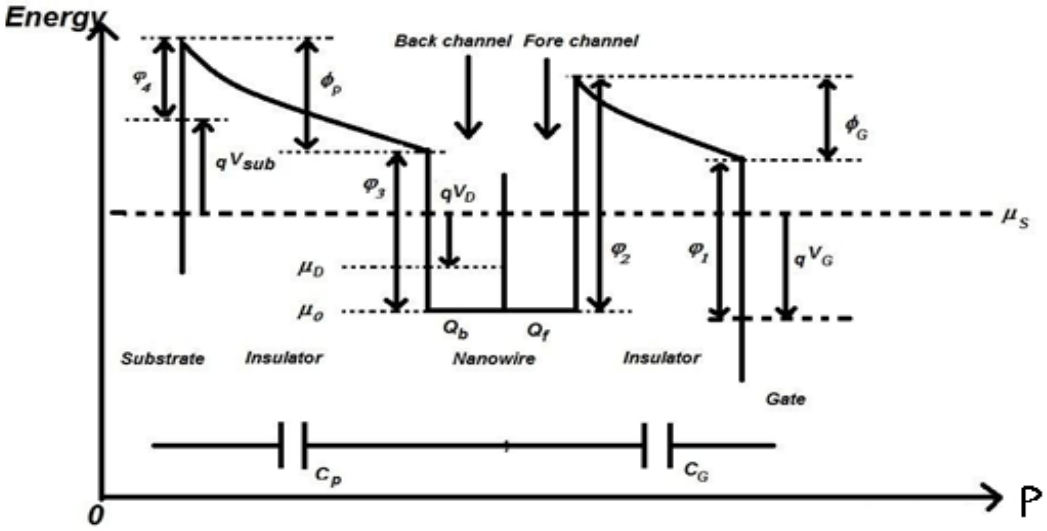

Figure 3.3: Potential energy diagram associated with the nanowire channel and nearby electrodes.

In cylindrical co-ordinate system there are three axes, ρ, θ, Z. In this co-ordinate system, the Schrodinger equation is represented in terms of equation (4) [43].

$$\frac{1}{\rho}\frac{\partial}{\partial\rho}\left(\rho\frac{\partial\Psi}{\partial\rho}\right)+\frac{1}{\rho^2}\frac{\partial^2\Psi}{\partial\theta^2}+\frac{\partial^2\Psi}{\partial Z^2}+\frac{2M}{\hbar^2}E\Psi=0 \ldots\ldots(4)$$

Where, $\Psi$is the wave function, E= Eigen values of energy, M= Effective mass which is 0.19 m_0 (m_0 = electron mass). Ψcan be expressed as

$$\Psi(\rho,\theta,Z)=\varphi(\rho,Z)\phi(\theta) \ldots\ldots\ldots\ldots(5)$$

Where,

$$\phi(\theta)=\frac{1}{\sqrt{2\pi}}e^{il\theta} \ldots\ldots\ldots(6)$$

and here l is the angular momentum quantum number and the values of l are 0, ±1, ±2,…...

$$\varphi(\rho,Z)=Ae^{ikz}\varrho(\rho) \ldots\ldots\ldots(7)$$

Where k is the wave number and can be expressed as

$$k=\sqrt{\frac{2ME}{\hbar^2}} \ldots\ldots\ldots\ldots(8)$$

If we substitute equations (5), (6) and (7) in equation (4), we will get the differential equation (9).

$$\frac{d^2\varrho}{d\rho^2} + \frac{1}{\rho}\frac{d\varrho}{d\rho} + \left(k^2 - \frac{l^2}{\rho^2}\right)\varrho = 0 \ldots\ldots\ldots (9)$$

If we solve equation (9), we will find $\varrho(\rho) = J_{|m|}(k\rho)$ where $J_{|m|}(k\rho)$ is Bessel function of m^{th} order. The n^{th} zero of the m^{th} Bessel function can be labelled as $a_{(m, n_\rho)}$. Considering the boundary condition $J_{|m|}(kR) = 0$, where $kR = a_{(m, n_\rho)}$, we finally get the energy which is shown in equation (10) [44].

$$E = \frac{\hbar^2}{2MR^2}[a_{(m, n_\rho)}]^2 \ldots\ldots\ldots (10)$$

Where R is the radius of the nanowire. The range of the radii that we chose was from 3nm to 10nm. After finding the eigen energies, the values were used in the drain current equation (2) along with the values of μ_S and μ_D considering the conduction band to be the reference and the structure to be intrinsic. Our results and their plots will be discussed in the next chapter.

Chapter 4 : Analysis of Results

4.1 Results and discussion

In our work we have analyzed the effect of width variation of a gate-all-around cylindrical SiNW MOSFET on a few important parameters using the analytical model discussed in section-3.3 [24]. As mentioned earlier, the current-voltage relationship curves i.e. the drain current versus drain voltage plots and the drain current versus gate voltage plots were used to determine the value of parameters at different radius. The parameters include- saturation current (I_S), saturation current density (J_S), sub-threshold swing (SS) and the peak of the transconductance (g_m).

At first, with the help of the equation-(2), we have reproduced figure-5 of [24]. Figure-4.1 shows that plot. We have used all the given values of the parameters from [24], and worked with only two of the lowest sub band energy levels.

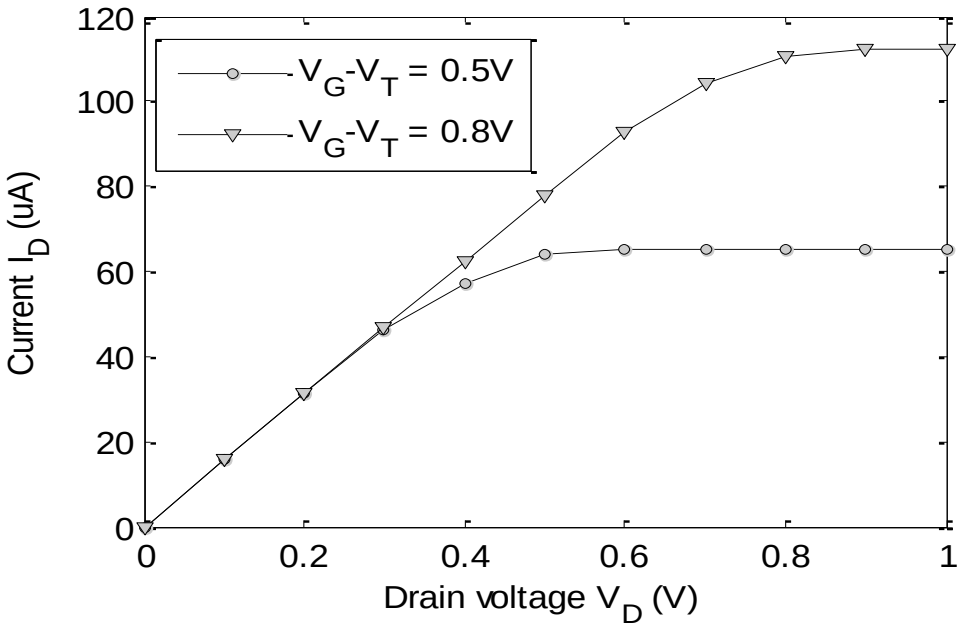

Figure 4.1: I_D-V_D characteristics for a Si nanowire MOSFET, reproduced from [24].

In figure-4.1, the device has threshold voltage, V_T=0.1V. The values of energy subbands we considered here are for i= 0, 1 in E_{i0} with E_{00}=0 and E_{10}=0.16eV [24]. E_{00} and E_{10} are the lowest two subband energies. Figure-4.1 contains the plot for two different gate overdrives.

Next, in figure-4.2, we have reproduced figure-6 from [24] and observed the characteristics.

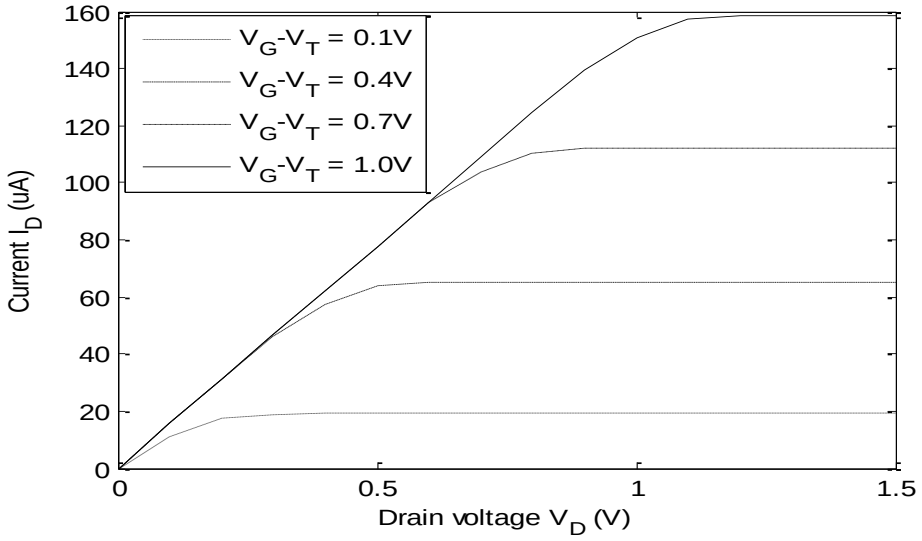

Figure 4.2: I_D-V_D characteristics for a Si nanowire MOSFET, reproduced from [24].

Figure-4.2 shows the I_D-V_D characteristics and the parameter is gate overdrive. As we can see in the figure that we have considered four different gate overdrives in this plot. We considered the threshold voltage here is 0.1V. In this figure we can see that the I_D-V_D characteristics are similar to those of a conventional MOSFET. This helped us determine the saturation current I_S (µA).

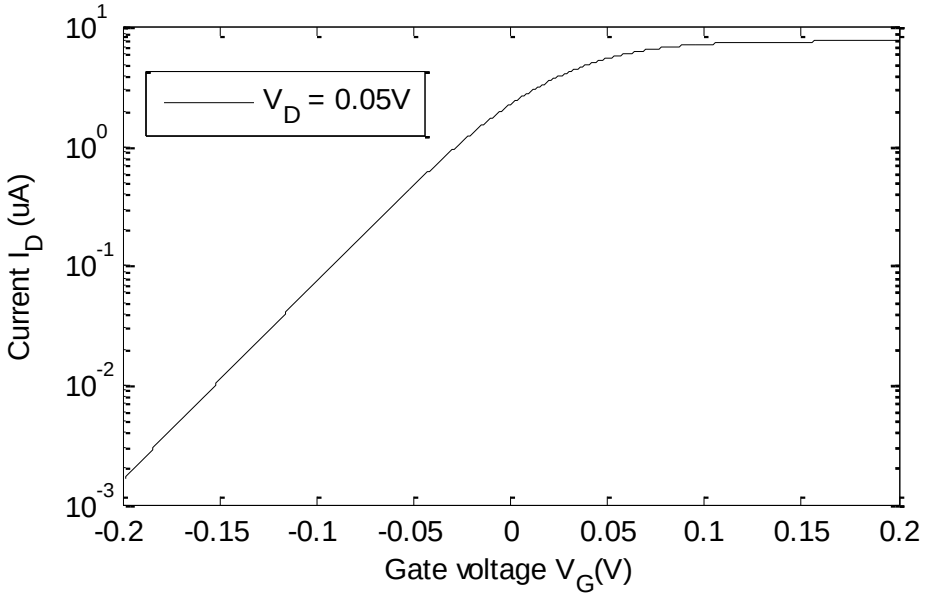

Figure 4.3: I_D-V_G characteristics for a Si nanowire MOSFET, reproduced from [24].

In figure-4.3, I_D-V_G characteristic of a Si nanowire MOSFET (nMOS) is plotted in logarithmic scale for a drain voltage of 50mV, in order to determine the sub threshold swing.

In the sub-threshold region, i.e. below V_T, I_D increase exponentially with V_G due to the energetic distribution of electrons in the conduction band of the semiconductor. Here, I_D is limited by thermionic emission above the energy barrier induced by the gate voltage. The exponential increase is described by the inverse sub-threshold slope. Sub-threshold swing is deduced from the transfer characteristics in the region with the highest slope on the logarithmic scale (figure-4.3). According to our calculation, the sub-threshold swing (SS) is 60mV/decade.

Figure-4.4 shows the variation of drain current as a function of gate voltage, where drain voltage was biased at 50 mV. In figure-4.3 I_D is plotted on a logarithmic scale and in figure-4.4 I_D is plotted on a linear scale to illustrate different aspects of the switching from the OFF-state at low V_G to the ON-state at high V_G. Alternatively, the transfer characteristic shows the V_G dependence of the transconductance, g_m.

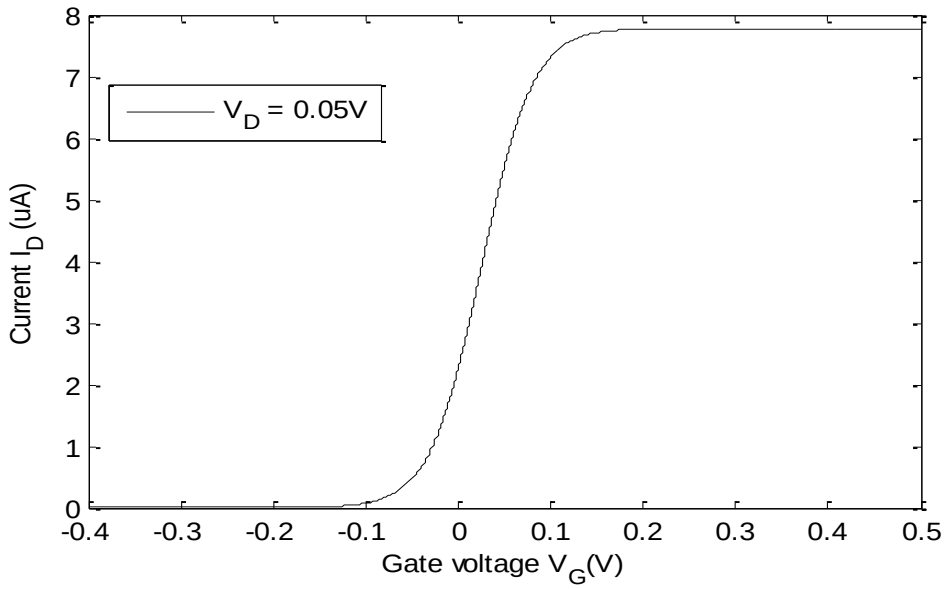

Figure 4.4: Drain Current variation as a function of the gate voltage.

The threshold voltage, V_T is also determined from drain current versus gate voltage plot i.e. from figure-4.4. The threshold voltage, V_T, is defined as the gate voltage at which the transistor switches between the ON-state and OFF-state. To extract V_T from experimental data, a support

line may be drawn which is the tangent of I_D at the V_G corresponding to peak g_m. V_T is the voltage where support line intersects with the x-axis.

The peak of the transconductance curve is determined from figure-4.5. The definition of the transconductance is $g_m = dI_D/dV_G$, this implies the ratio of the drain current change to the gate voltage change. Transconductance, g_m is an important metric for the speed of the transistor and is often represented by its peak value. The peak value here is 69.52μA/V.

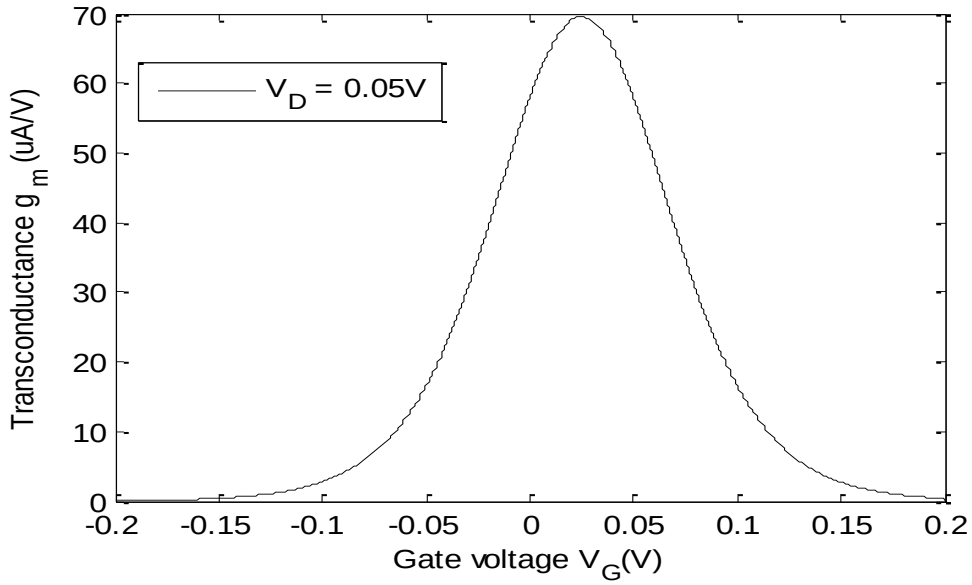

Figure 4.5: Transconductance variation as a function of the gate voltage.

We have calculated drain current, transfer characteristics and transconductance for radii of 3nm to 10 nm. For the previous plots (i.e. for figure-4.1 to figure-4.5), there were just two energy subbands given in [24], which were insufficient for our work. We had to investigate the effect of width variation on parameters, so we needed more energy levels. For this work, we generated eigen energy values by substituting the solution of the Bessel's equation in equation-(3). We had to solve Schrodinger's equation to get the solution of the Bessel's function. We generated energy values of eigenstates for certain radii of a cylindrical SiNW MOSFET. The plots we have drawn for different radii are given below. For instance we have plotted the figures for radius 3nm, 6nm and 10nm. We have calculated till the 6^{th} zero of the 4^{th} Bessel function and chosen all the energy values which are less than 1eV. The tables that contain the energies are included in Appendix-A.

The plots for radius, R=3nm are given below. These plots contain I_D-V_D, transfer characteristics and transconductance.

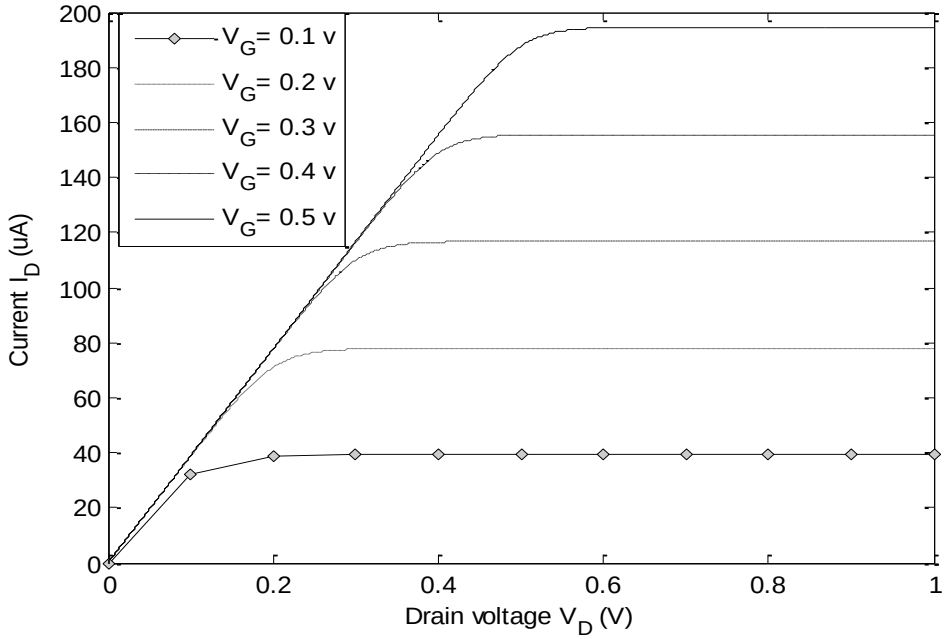

Figure 4.6: I_D-V_D characteristics for a Si nanowire MOSFET, for different gate voltages at radius 3nm.

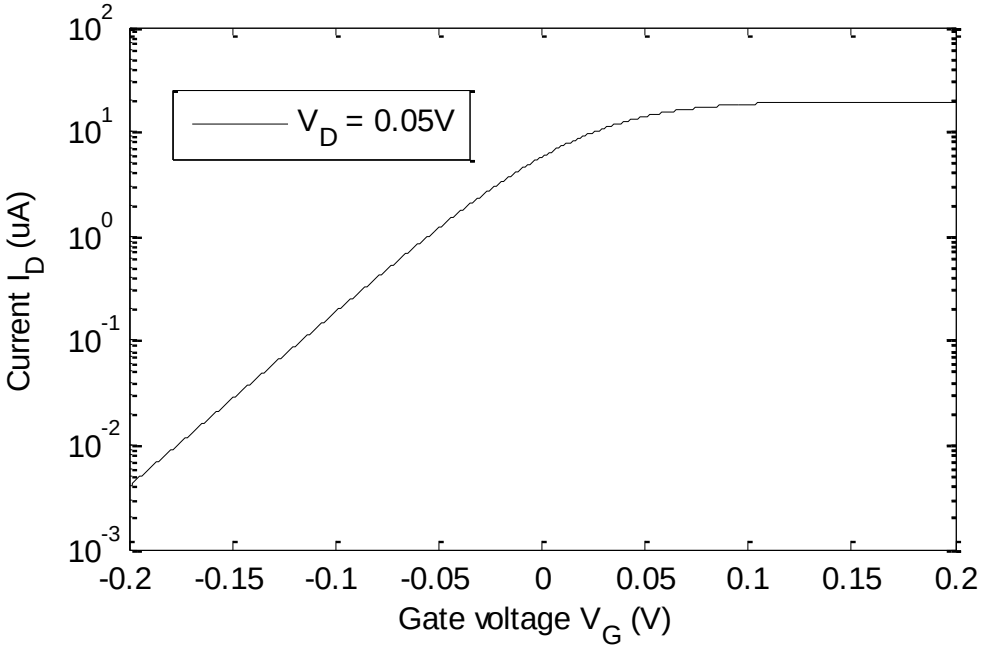

Figure 4.7: I_D-V_G characteristics for a Si nanowire MOSFET, in logarithmic scale at radius 3nm.

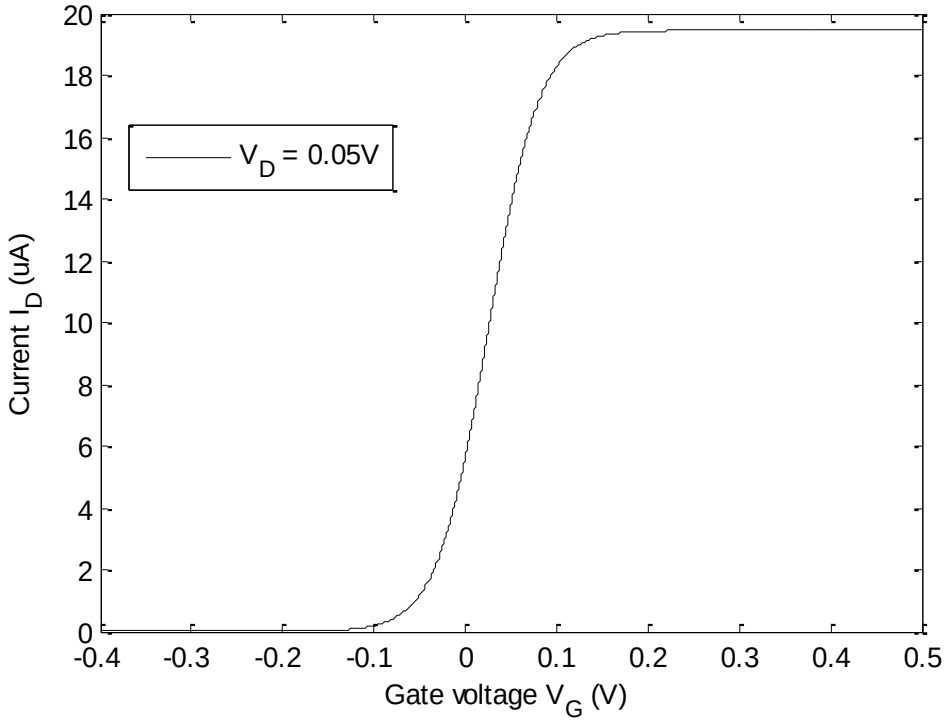

Figure 4.8: Drain Current variation as a function of the gate voltage at radius 3nm.

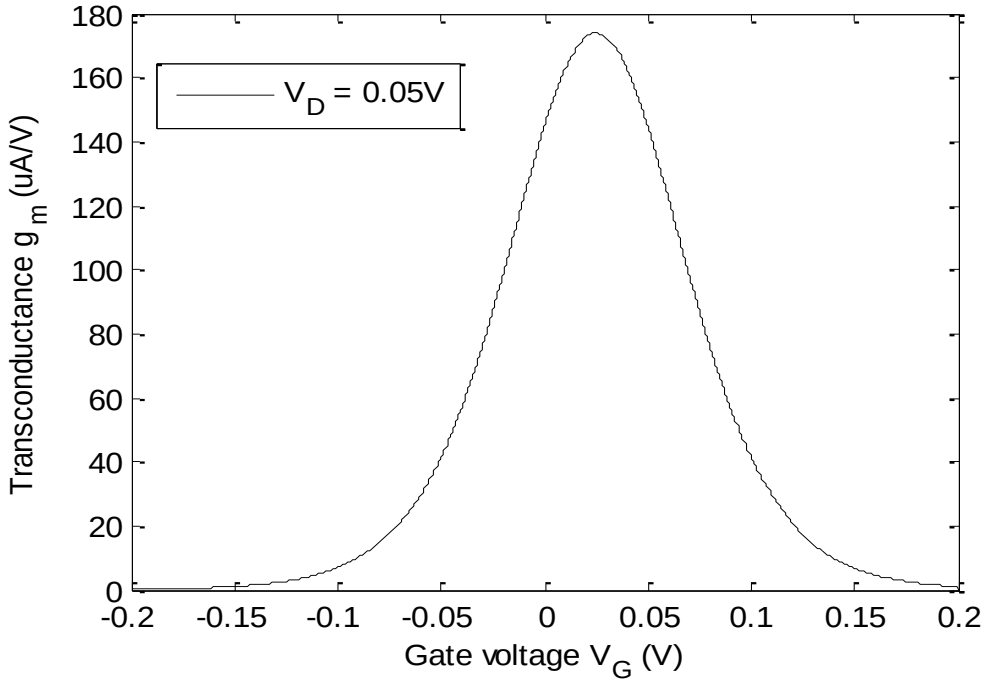

Figure 4.9: Transconductance variation as a function of the gate voltage at radius 3nm.

The plots for radius, R=6nm are given below. These plots contain I_D-V_D, transfer characteristics and transconductance.

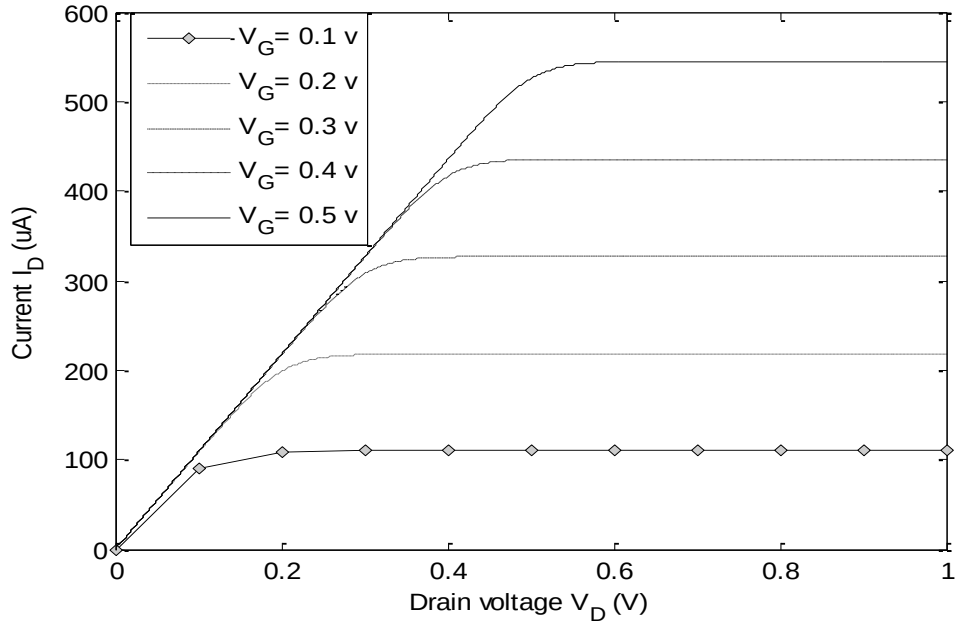

Figure 4.10: I_D-V_D characteristics for a Si nanowire MOSFET, for different gate voltages at radius 6nm.

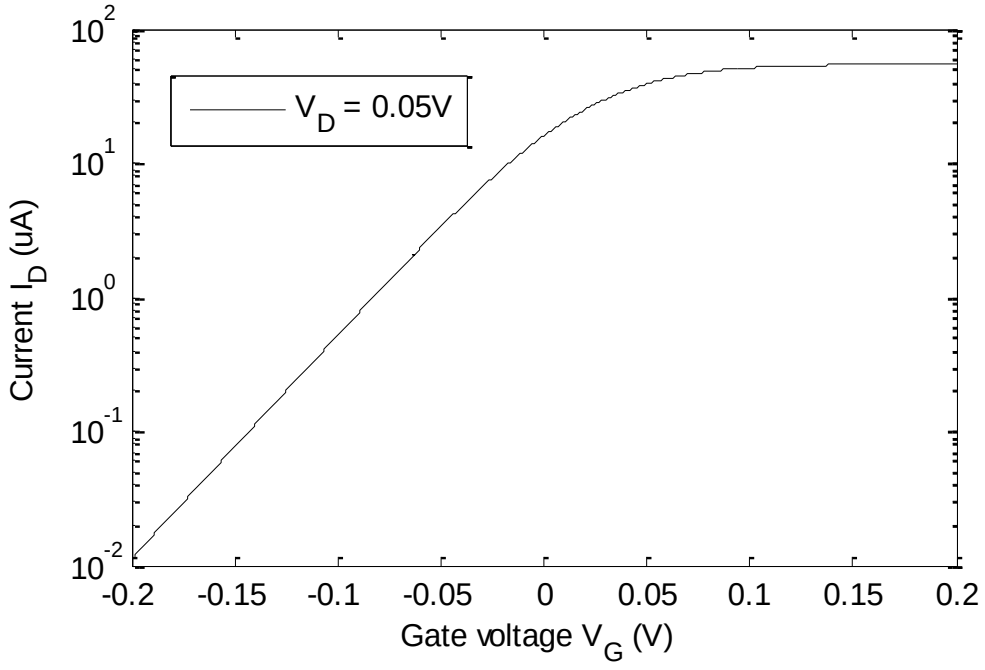

Figure 4.11: I_D-V_G characteristics for a Si nanowire MOSFET, in logarithmic scale at radius 6nm.

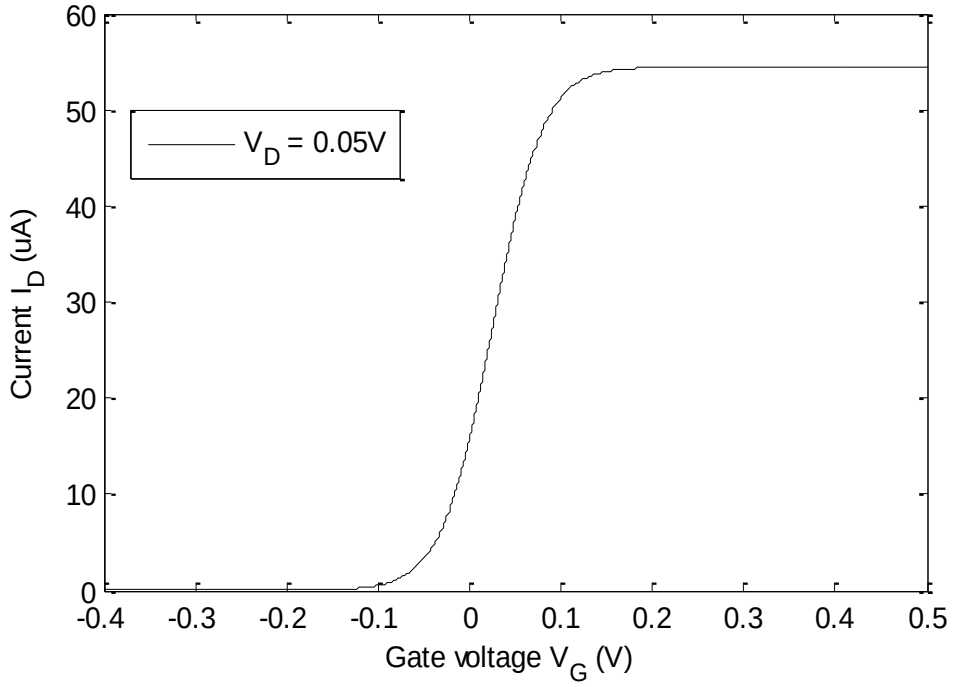

Figure 4.12: Drain Current variation as a function of the gate voltage at radius 6nm.

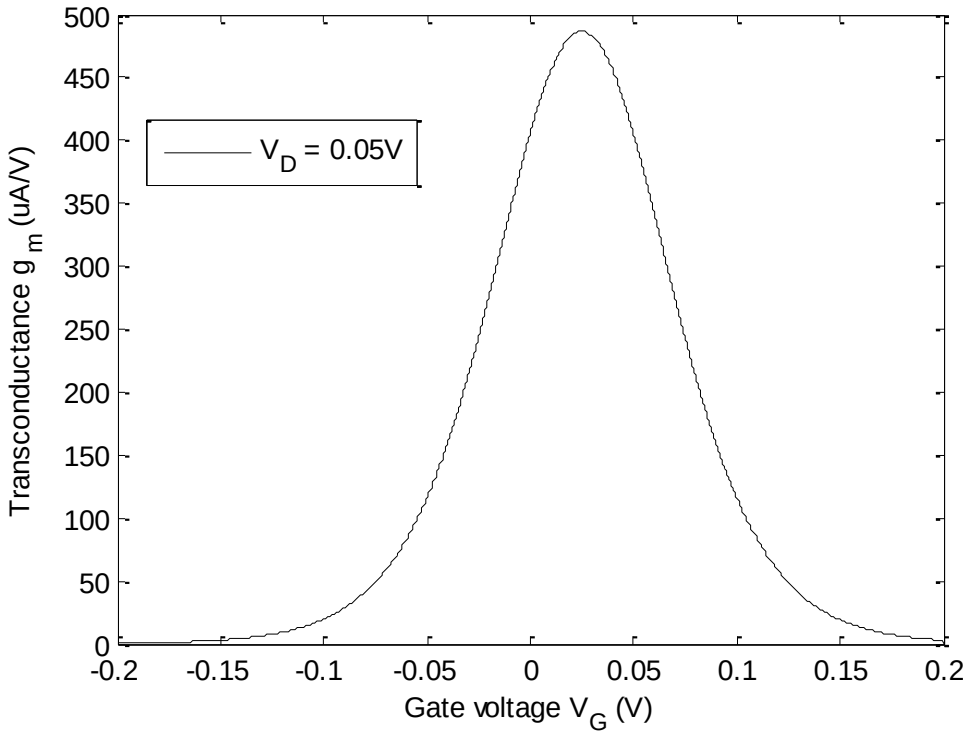

Figure 4.13: Transconductance variation as a function of the gate voltage at radius 6nm.

The plots for radius, R=10nm are given below. These plots contain I_D-V_D, transfer characteristics and transconductance.

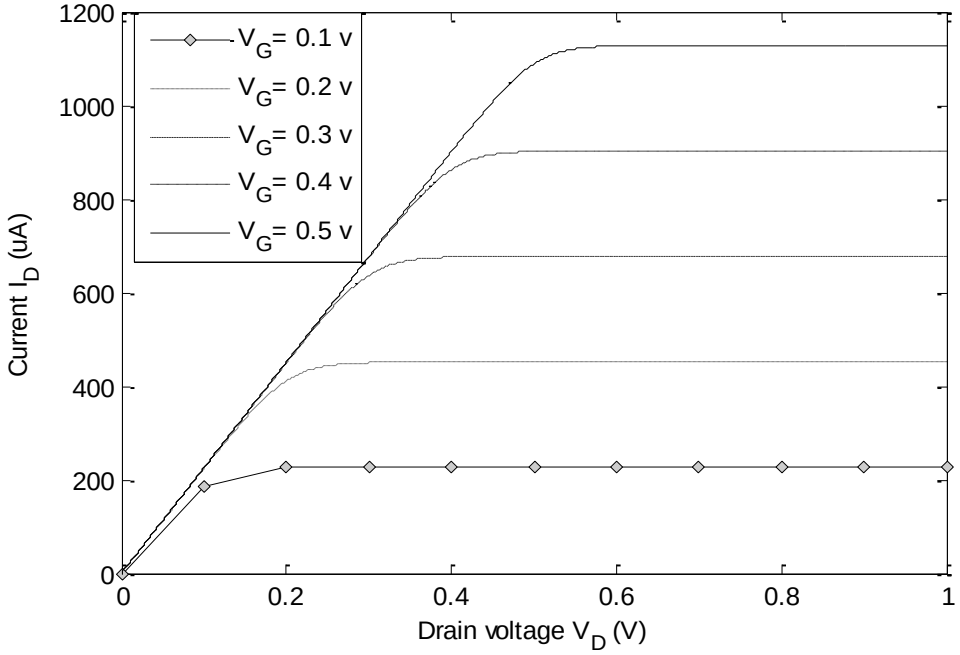

Figure 4.14: I_D-V_D characteristics for a Si nanowire MOSFET, for different gate voltages at radius 10nm.

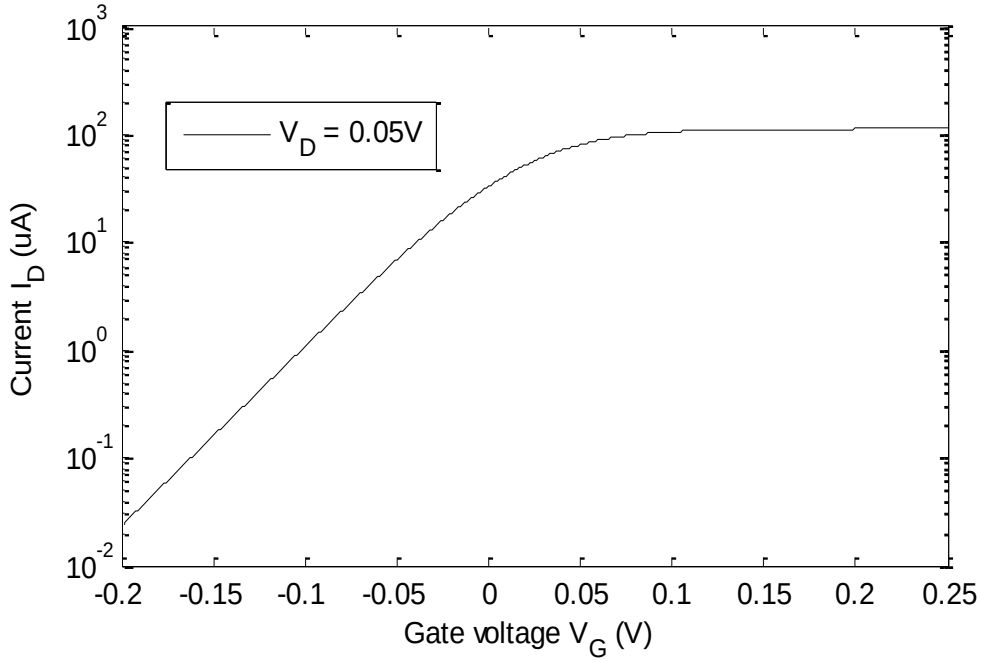

Figure 4.15: I_D-V_G characteristics for a Si nanowire MOSFET, in logarithmic scale at radius 10nm.

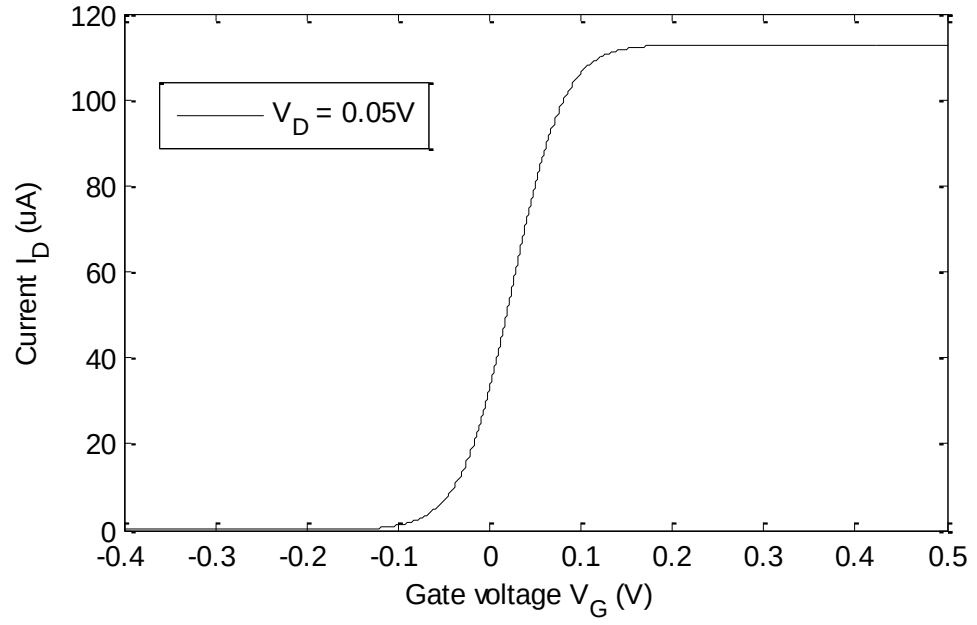

Figure 4.16: Drain Current variation as a function of the gate voltage at radius 10nm.

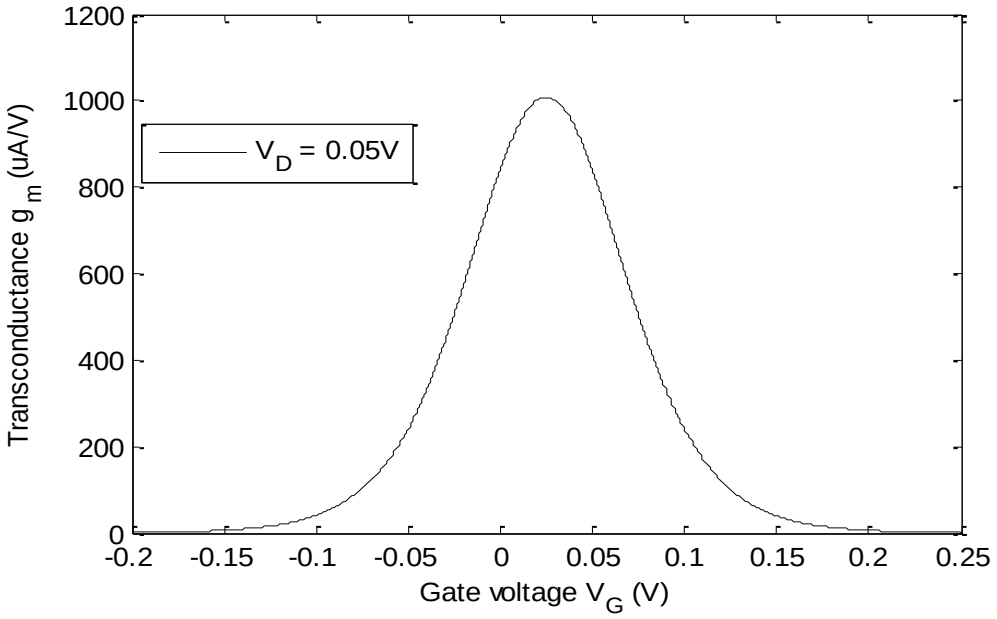

Figure 4.17: Transconductance variation as a function of the gate voltage at radius 10nm.

From all the above figures it is clear that the value of some parameters will differ at different radius, though some parameters values may remain unchanged. The tables containing the values of the parameters for radii of 3nm to 10nm are included in Appendix-B.

4.2 Comparison of results

The derived values of parameters represented in plots with the change in radius, are given below.

Saturation current (I_S): In our report, the saturation current (I_S) variation versus radius (R) is evaluated with the gate voltage of 0.3V and the drain voltage of 1V.

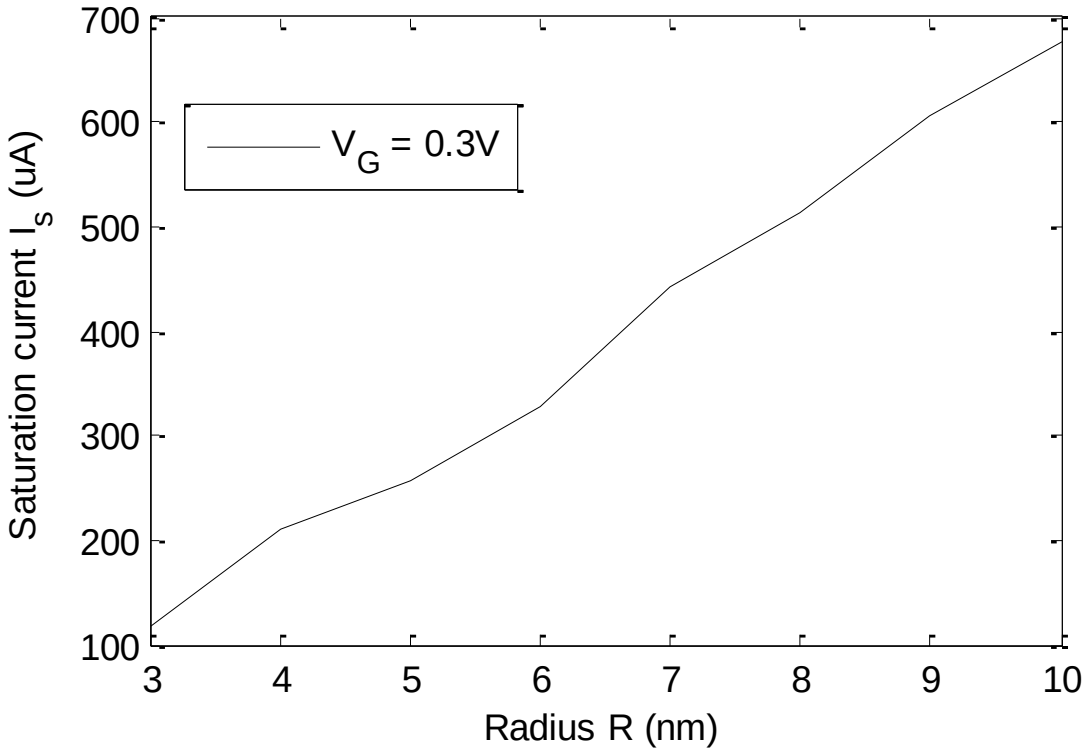

Figure 4.18: Change of saturation current (I_S), with the change in radius (R).

Figure-4.18 shows the change of saturation current with the change in radius for the n-channel FET. The Si nanowire with a large radius has high drain current. That means Saturation Current (I_S) is dependent on radius and saturation current increases with increasing channel thickness.

Saturation current density (J_S) is given by $J_S = I_S/(\text{area of NW})$. By calculating the cross sectional area of a gate all around cylindrical Si nanowire we can determine J_S. The table containing the values of saturation current density is included in Appendix-C. If we observe the results of saturation current density (J_S) for radii of 3-10nm, we can see the variation of J_S with increasing radius. For radius, R=3nm we found $J_S(3nm) = 4.127 \mu A/nm^2$ and for radius, R= 10nm,

J_S(10nm)= 2.154μA/nm^2. This implies that the saturation current density is higher in narrower wires. This is one of the motivations to make the NW narrow.

Sub-threshold swing (SS): Figure-4.19 represents the variation of sub-threshold swing (SS) with different radius (R).

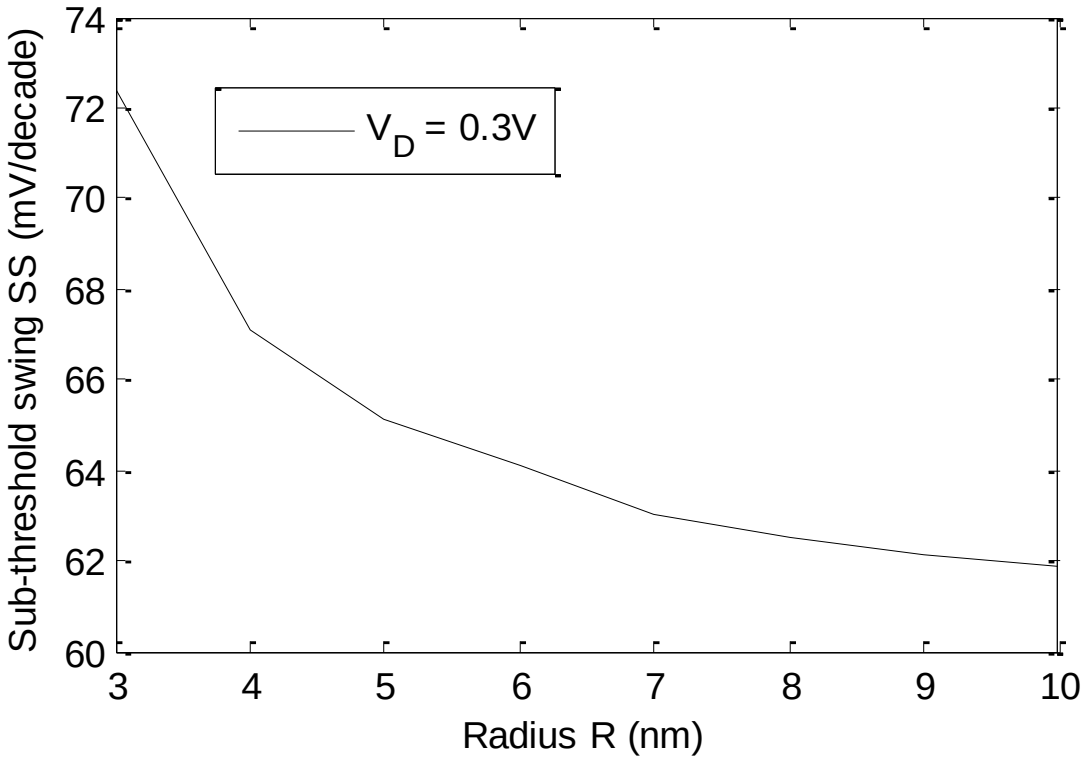

Figure 4.19: Change of sub-threshold swing (SS), with the change in radius (R).

In figure-4.19 the plot shows that, the value of sub-threshold swing decreases with increasing value of radius. For lowest radius (3nm) the Sub-threshold Swing (SS) shows highest value and decreases gradually with increasing radius.

Transconductance (g_m): In our work we have observed the change in the peak of transconductance (g_m), with changing radius, which is drawn in figure-4.20.

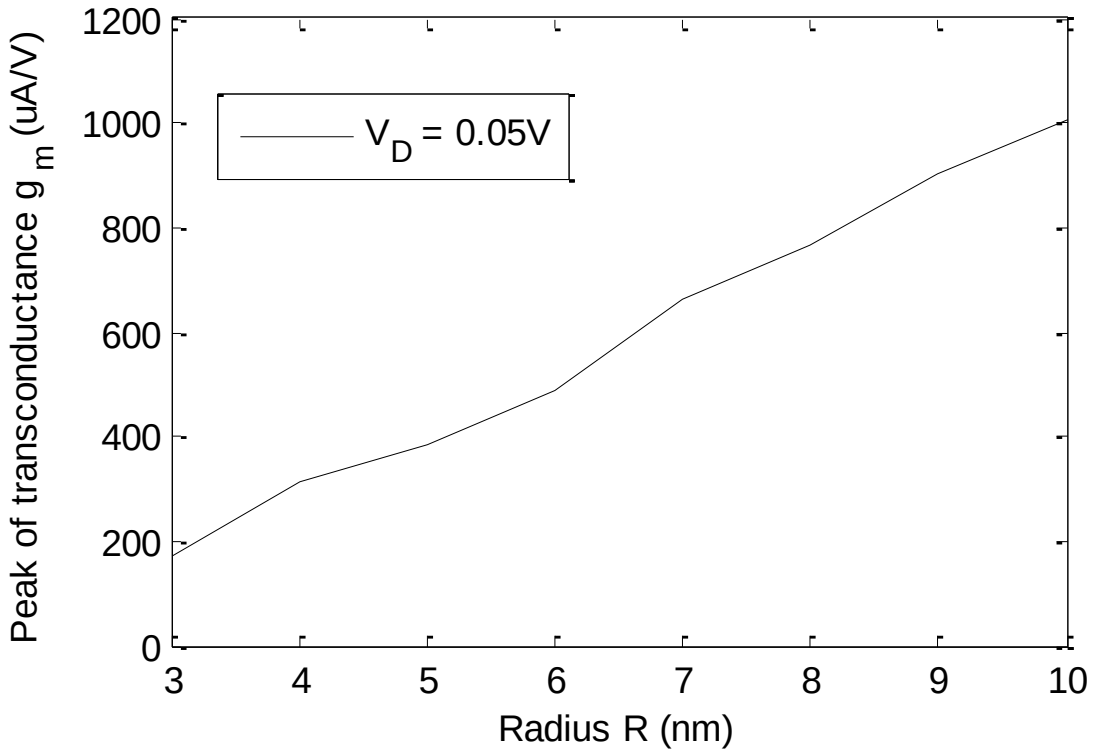

Figure 4.20: Change of peak transconductance (g_m), with the change in radius (R).

This figure shows an increment from lowest radius to its highest. From investigating the plot it can be said that the peak of transconductance (g_m) value increases with increasing radius.

Chapter 5 : Summary

5.1 Conclusion

The objective of this work is to analyze the effect of wire width variation on different parameters of a Si nanowire MOSFET. For this purpose, we used the model used by Natori [24]. This model is used to obtain the current voltage relationship of ballistic nanowire MOSFETs for certain given energy levels. To analyze the effect of width variation Bessel's function is used to get Eigen energies for required radii. MATLAB code is used to extract energy values from equation as per need.

After we observed the effect of width variation on saturation current (I_S) we found that the saturation current increases with width. That means wider channel gives a higher amount of saturation current. When we observed the effect of saturation current density (J_S), we found saturation current density (J_S) increases with decreasing nanowire radius. This indicates that, the scaling or downsizing of nanowires has positive impact in terms of power. Moving on to the sub threshold swing (SS) we found a decrease in the value, with respect to increase in radii. At last we observed the peak of transconductance (g_m) with the change in radius. In this part we have got an increment in peak of transconductance (g_m), with the increment in radius (R).

5.2 Future works

In our study the discussion is only limited to observation of the characteristics of saturation current, saturation current density, sub threshold slope and the peak of transconductance with varying radii. Further scope of work may involve more complex issues. As the nanowire becomes smaller the short channel effect (SCE) becomes severe. So, the SCE can be included in the model. Throughout our work, we have considered the threshold voltage to be 0V for determining the I_D-V_G characteristics for radii of 3-10nm. In order to observe the trend of the threshold voltage with varying radii, in future works we may investigate the variation of the threshold voltage. In our work we have assumed the MOSFET to be ballistic and so the mobility concept does not apply. So, future work may be done with a non-ballistic MOSFET. In a non-ballistic MOSFET the mobility effects can be included. This report discusses only the DC effects; in future works RF effects can be included. Under RF effects, the effect of width variation in gate capacitance and parasitic capacitance can also be involved in the extension of

future works. Besides, comparison between other models can be made to have a better idea of the accuracy of the model.

Appendix

Appendix - A

Table A-1: The values of eigen energies E (eV) for R= 3nm.

	n=0	n=1	n=2	n=3	n=4	n=5	n=6
m=0	0.1290	0.6797	1.6705	3.1016	4.9730	7.2848	10.0368
m=1	0.3275	1.0979	2.3086	3.9600	6.0515	8.5835	11.5557
m=2	0.5884	1.5805	3.0120	4.8835	7.1953	9.9474	13.1398
m=3	0.9081	2.7310	3.7788	5.8713	8.4037	11.3762	14.7894
m=4	1.2845	2.1254	4.6080	6.9225	9.6760	12.8693	16.5027

Table A-2: The values of eigen energies E (eV) for R= 4nm.

	n=0	n=1	n=2	n=3	n=4	n=5	n=6
m=0	0.0726	0.3824	0.9397	1.7446	2.7973	4.0977	5.6457
m=1	0.1842	0.6176	1.2987	2.2275	3.4040	4.8282	6.5001
m=2	0.3309	0.8890	1.6942	2.7470	4.0474	5.5954	7.3912
m=3	0.5108	1.1955	2.1255	3.3026	4.7271	6.3991	8.3190
m=4	0.7225	1.5362	2.5920	3.8939	5.4428	7.2390	9.2828

Table A-3: The values of eigen energies E (eV) for R= 5nm.

	n=0	n=1	n=2	n=3	n=4	n=5	n=6
m=0	0.0464	0.2447	0.6014	1.1166	1.7903	2.6225	3.6132
m=1	0.1179	0.3953	0.8312	1.4256	2.1786	3.0901	4.1600
m=2	0.2118	0.5690	1.0843	1.7581	2.5903	3.5811	4.7303
m=3	0.3269	0.7651	1.3604	2.1137	3.0253	4.0954	5.3242
m=4	0.4624	0.9832	1.6589	2.4921	3.4834	4.6330	5.9410

Table A-4: The values of eigen energies E (eV) for R= 6nm.

	n=0	n=1	n=2	n=3	n=4	n=5	n=6
m=0	0.0323	0.1699	0.4176	0.7754	1.2433	1.8212	2.5092
m=1	0.0819	0.2745	0.5772	0.9900	1.5129	2.1459	2.8889
m=2	0.1471	0.3951	0.7530	1.2209	1.7988	2.4869	3.2850
m=3	0.2270	0.5313	0.9447	1.4678	2.1009	2.8441	3.6973
m=4	0.3211	0.6828	1.1520	1.7306	2.4190	3.2173	4.1257

Table A-5: The values of eigen energies E (eV) for R= 7nm.

	n=0	n=1	n=2	n=3	n=4	n=5	n=6
m=0	0.0237	0.1248	0.3068	0.5697	0.9134	1.3380	1.8435
m=1	0.0602	0.2017	0.4241	0.7273	1.1115	1.5766	2.1225
m=2	0.1081	0.2903	0.5532	0.8970	1.3216	1.8271	2.4134
m=3	0.1668	0.3904	0.6941	1.0784	1.5435	2.0895	2.7164
m=4	0.2359	0.5016	0.8464	1.2715	1.7772	2.3638	3.0311

Table A-6: The values of eigen energies E (eV) for R= 8nm.

	n=0	n=1	n=2	n=3	n=4	n=5	n=6
m=0	0.0181	0.0956	0.2349	0.4362	0.6993	1.0244	1.4114
m=1	0.0461	0.1544	0.3247	0.5569	0.8510	1.2071	1.6250
m=2	0.0827	0.2223	0.4236	0.6867	1.0118	1.3989	1.8478
m=3	0.1277	0.2989	0.5314	0.8257	1.1818	1.5998	2.0798
m=4	0.1806	0.3841	0.6480	0.9735	1.3607	1.8098	2.3207

Table A-7: The values of eigen energies E (eV) for R= 9nm.

	n=0	n=1	n=2	n=3	n=4	n=5	n=6
m=0	0.0143	0.0755	0.1856	0.3446	0.5526	0.8094	1.1152
m=1	0.0364	0.1220	0.2565	0.4400	0.6724	0.9537	1.2840
m=2	0.0654	0.1756	0.3347	0.5426	0.7995	1.1053	1.4600
m=3	0.1009	0.2362	0.4199	0.6524	0.9337	1.2640	1.6433
m=4	0.1427	0.3034	0.5120	0.7692	1.0751	1.4299	1.8336

Table A-8: The values of eigen energies E (eV) for R= 10nm.

	n=0	n=1	n=2	n=3	n=4	n=5	n=6
m=0	0.0116	0.0612	0.1503	0.2791	0.4476	0.6556	0.9033
m=1	0.0295	0.0988	0.2078	0.3564	0.5446	0.7725	1.0400
m=2	0.0530	0.1422	0.2711	0.4395	0.6476	0.8953	1.1826
m=3	0.0817	0.1913	0.3401	0.5284	0.7563	1.0239	1.3310
m=4	0.1156	0.2458	0.4147	0.6230	0.8708	1.1582	1.4852

Appendix - B

Table B-1: Data derived from plots for R= 3nm.

Data derived from I - V_D plot					
Gate Overdrive, V_G (V)	0.1	0.2	0.3	0.4	0.5
Saturation Current, I_S (µA)	39.06	77.80	116.7	155.6	194.5
Data derived from I - V_G plot					
Drain Bias, V_D (V)	0.05		0.1	0.3	0.6
Sub-threshold Swing, SS (mV/decade)			72.4		
Peak of transconductance (µA/ V)	173.8				

Table B-2: Data derived from plots for R= 4 nm.

Data derived from I - V_D plot					
Gate Overdrive, V_G (Volt)	0.1	0.2	0.3	0.4	0.5
Saturation Current, I_S (µA)	70.26	139.7	210	280.1	350.1
Data derived from I - V_G plot					
Drain Bias, V_D (Volt)	0.05		0.1	0.3	0.6
Sub-threshold Swing, SS (mV/decade)			67.1		
Peak of transconductance (µA/ V)	312.9				

Table B-3: Data derived from plots for R= 5 nm.

Data derived from I - V_D plot					
Gate Overdrive, V_G (Volt)	0.1	0.2	0.3	0.4	0.5
Saturation Current, I_S (µA)	85.92	171.1	256.6	342.3	427.6
Data derived from I - V_G plot					
Drain Bias, V_D (Volt)	0.05		0.1	0.3	0.6
Sub-threshold Swing, SS (mV/decade)			65.1		
Peak of transconductance (µA/ V)	382.4				

Table B-4: Data derived from plots for R= 6 nm.

Data derived from I - V_D plot					
Gate Overdrive, V_G (Volt)	0.1	0.2	0.3	0.4	0.5
Saturation Current, I_S (µA)	109	217.7	326.7	435.6	544.6
Data derived from I - V_G plot					
Drain Bias, V_D (Volt)	0.05		0.1	0.3	0.6
Sub-threshold Swing, SS (mV/decade)			64.1		
Peak of transconductance (µA/ V)	486.7				

Table B-5: Data derived from plots for R= 7 nm.

Data derived from I - V_D plot					
Gate Overdrive, V_G (Volt)	0.1	0.2	0.3	0.4	0.5
Saturation Current, I_S (µA)	148.1	295.4	443.1	591.2	738.9
Data derived from I - V_G plot					
Drain Bias, V_D (Volt)	0.05		0.1	0.3	0.6
Sub-threshold Swing, SS (mV/decade)			63		
Peak of transconductance (µA/ V)	660.5				

Table B-6: Data derived from plots for R= 8 nm.

Data derived from I - V_D plot					
Gate Overdrive, V_G (Volt)	0.1	0.2	0.3	0.4	0.5
Saturation Current, I_S (µA)	171.9	342.3	513.5	684.6	855.8
Data derived from I - V_G plot					
Drain Bias, V_D (Volt)	0.05		0.1	0.3	0.6
Sub-threshold Swing, SS (mV/decade)			62.5		
Peak of transconductance (µA/ V)	764.7				

Table B-7: Data derived from plots for R= 9 nm.

Data derived from I - V_D plot					
Gate Overdrive, V_G (Volt)	0.1	0.2	0.3	0.4	0.5
Saturation Current, I_S (µA)	202.4	404.4	606.7	809	1011
Data derived from I - V_G plot					
Drain Bias, V_D (Volt)	0.05		0.1	0.3	0.6
Sub-threshold Swing, SS (mV/decade)			62.1		
Peak of transconductance (µA/ V)	903.9				

Table B-8: Data derived from plots for R= 10 nm.

Data derived from I - V_D plot					
Gate Overdrive, V_G (Volt)	0.1	0.2	0.3	0.4	0.5
Saturation Current, I_S (µA)	226.2	451	676.7	902.3	1128
Data derived from I - V_G plot					
Drain Bias, V_D (Volt)	0.05		0.1	0.3	0.6
Sub-threshold Swing, SS (mV/decade)			61.9		
Peak of transconductance (µA/ V)	1008				

Appendix - C

Table C-1: Variation of Saturation current (I_S) and saturation current density (J_S) with radius.

Radius R (nm)	Saturation current I_S (μA)	Saturation current density J_S (μA/ nm^2)
3	116.7	4.127
4	210.0	4.178
5	256.6	3.267
6	326.7	2.889
7	443.1	2.878
8	513.5	2.554
9	606.7	2.384
10	676.7	2.154

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