East West University

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Process simulation of FILOX vertical MOSFET to estimate fabrication parameters.

By

Tarikul Islam Milon

(ID: 2011-3-80-014)

And

Kousar Hossain

(ID: 2011-3-80-022)

And

Fara Jannat Shova

(ID: 2011-3-80-023)

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Approved By

Thesis Advisor	Department Chairperson
Dr. Mohammad Mojammel AL Hakim	Dr. Muhammed Mazharul Islam

Approval

The thesis title "Process simulation of FILOX vertical MOSFET to estimate fabrication parameters" submitted by Tarikul Islam Milon [2011-3-80-014], Kousar Hossain [2011-3-80-022] and Fara Jannat Shova [2011-3-80-023] in the semester of fall-2015 is approved satisfactory in partial fulfillment of the requirements for the requirements for the degree of Bachelor of Science in Electrical and Electronics Engineering.

Dr. Mohammad Mojammel AL Hakim

Associate Professor, Department of Electrical and Electronics Engineering

East West University, Dhaka, Bangladesh

Declaration

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Tarikul Islam Milon

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Kousar Hossain

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Fara Jannat Shova

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ABSTRACT

The aim of this thesis work is to study the Process simulation of FILOX vertical MOSFET to estimate fabrication parameters for RF application. Double gate or surround-gate vertical metal oxide semiconductor field effect transistors is delayed by the parasitic overlap capacitance related with their layout, which is larger than for a lateral MOSFET on the same technology node. A simple self-aligned process has been developed to reduce the parasitic overlap capacitance in vertical MOSFETs using nitride spacers on the sidewalls of the trench or pillar and a local oxidation. In this thesis we describe different steps of FILOX vertical MOSFET fabrication and finally we get 115nm of channel length , 140nm of junction depth, 3.3nm of gate oxide thickness, 4×10^{18} cm^{-3} of body doping and 2×10^{20} cm^{-3} of source/drain doping in the FILOX vertical MOSFET. We also describe the parameters that required to be changed to obtain different desired body doping value for our FILOX vertical MOSFET. This thesis we observed that decrease in dose of p-type implantation causes a decrease in body doping but this also changes the channel length. Therefore, to obtain our targeted channel length 115nm and junction depth 140nm we have to decrease the energy too. Simultaneously, we slightly need to decrease the dose and energy of n-type implantation. To get the desired body doping we see the alteration of channel length 115nm and junction depth 140nm. Then we adjusted the dose and energy of FILOX vertical MOSFET.

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We wish to express our deepest gratitude to Md. Delowar Hossain and Md. Jakaria Yusuf Khan for helping us to solve some sophisticated theoretical problems during our thesis. Their helpful hand and friendly behavior made us happy and the thesis easy.

We are much obliged to our family for their support and love shown over the years for supporting us and helping us get through the difficult times.

AUTHORIZATION

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Tarikul Islam Milon

Kousar Hossain

Fara Jannat Shova

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1 CHAPTER: INRODUCTION

1.1 Motivation

In modern CMOS technology the MOSFETs has been scaled down in size. Small MOSFETs are desirable for several reasons. The main reason of making transistors small is to pack more devices in a smaller chip area. This results in a chip with more functionality in same area. It is expected that smaller transistors will provide faster operation. Scaling of the MOSFETs require all devices dimension to be reduced proportionally.

The device dimensions are channel length, Junction depth and gate oxide thickness. Due to scale down of the MOSFETs size when the channel length of MOSFETs is 115nm some operational problems occur which is known as short channel effect (SCE) including hot carrier effects, punch-through effect, velocity saturation effect etc. Moreover, the fabrication cost of conventional planar MOSFETs below 115nm channel lengths is extremely expensive due to expensive lithography requirement to define the channel region.

Many types of alternative architectures are investigated to eliminate the short channel effect and to reduce the MOS fabrication cost in conventional silicon based technology. Such as,

- FINFET.
- Planner double gate MOSFETs.
- and Vertical MOSFETs etc.

1.2 Vertical MOSFETs and its Background

Among these different device structures investigated vertical MOSFETs are potentially attractive due to following reasons.

1. Easier realization of surround gate structures.
2. Flexibility of designing short channel devices using relaxed lithography node.
3. Decoupling of the gate length from the packing density.
4. Less silicon area requirement to fabricate a vertical MOSFET

There have been several approaches investigated for designing and fabrication of vertical MOSFETs. These approaches are separated as three different types of vertical MOSFETs such as,

Type 1 - Vertical MOSFETs based on epitaxy.

Type 2 - Vertical replacement gate MOSFETs.

Type 3 - Vertical MOSFETs based on ion implantation.

1.2.1 Vertical MOSFETs based on epitaxy

A MOSFETs transistor of type 1, vertical MOSFETs based on epitaxy [1-5] is manufactured by accurately growing epitaxial layers for the heavily doped (n+) drain and source and p type channel illustrated in figure 1-1 For good control of channel length accurate epitaxy is needed. That can be achieved by using controlled low pressure chemical vapor deposition (LPCVD), to grow single crystal material on substrate. After epitaxy process a vertical MOSFETs transistor is manufactured by a pillar etch, gate oxide growth and finally a polysilicon gate is deposited and patterned. The main disadvantage of this technique is the integration of epitaxial layer into a standard CMOS process. Both source and drain extend across the full width of the pillar, this configuration gives very high parasitic bipolar transistor action. Another major disadvantage is the source/ drain overlap capacitance as polisilicon gate passes over the pillar top and bottom respectively for lithographic alignment tolerance and gate track to contact.

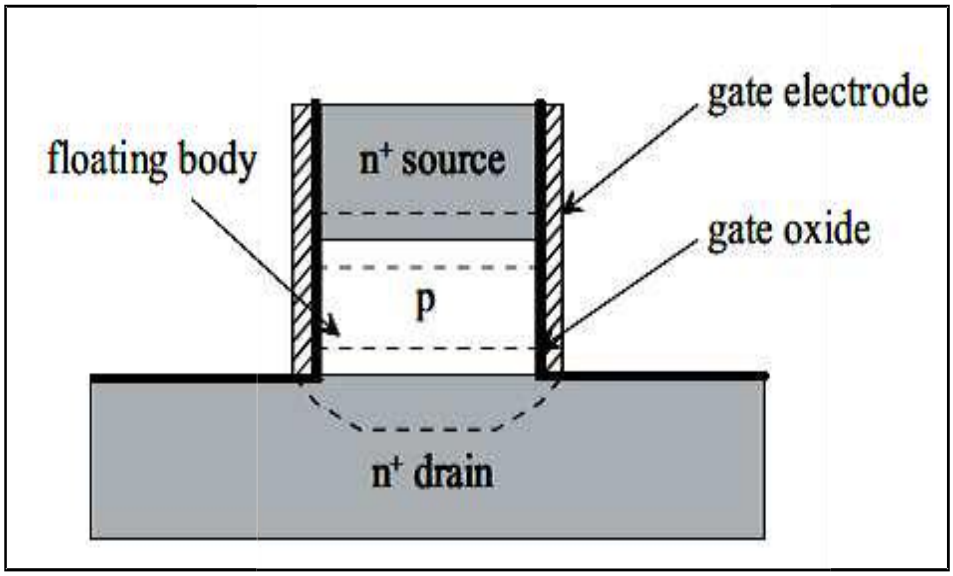

Figure 1-1:Vertical MOSFET based on epitaxy.

A variant of epitaxy approach has also been developed, which uses selective epitaxy [6-10] as illustrated in figure 1-2. In this approach, an oxide/ polysilicon/ oxide stock is created before the epitaxy. Then a trench is created by dry etches and gate oxide is grown. By using selective epitaxy the heavily doped (n^+), drain, source and p-type channel is created. This selective epitaxy removes overlap capacitance but high parasitic bipolar

gain remains problem. Moreover, other problems are creation of the high quality gate oxide on polysilicon and the controlling facets during selective capacity.

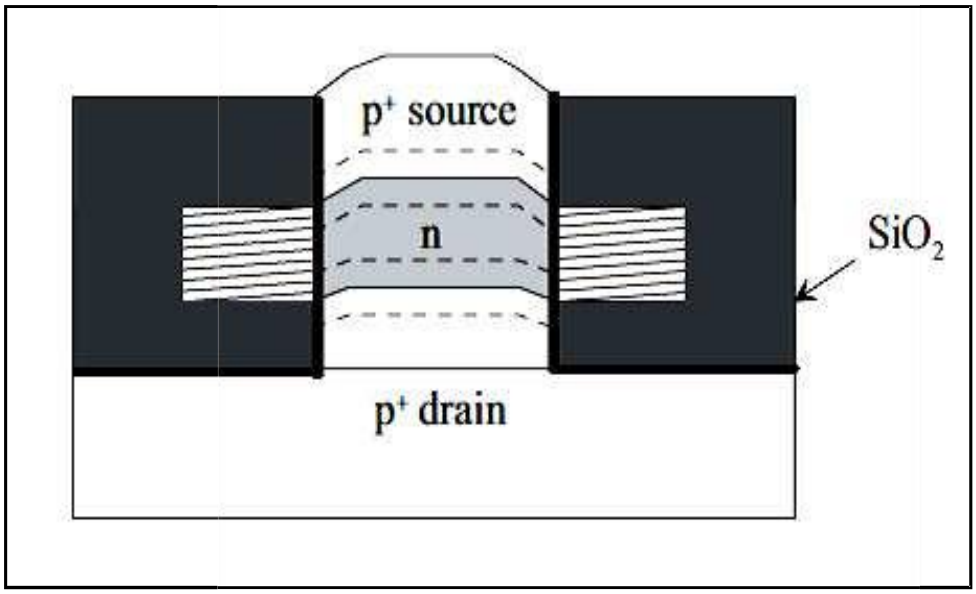

Figure 1-2:Vertical MOSFET based on selective epitaxy with reduced overlap capacitanc.

1.2.2 Vertical replacement gate MOSFETs

The type 2 vertical MOSFETs is shown the figure 1-3 that is the vertical replacement gate MOSFETs (VRG). The VRG MOSFETs [11-14] can be made with competitive parasitic capacitances and packing density as compare to planar MOSFETs. Here, the layer deposition method is used to create a channel length which defined by the layer thickness. The gate length is precisely defined by a blanket film deposition. At first, arsenic ion is implanted into silicon wafer to form heavily doped (n–) drain regions. Then multi-layer stack of phosphosilicate glass (PSG)/ nitride/ undoped oxide/ nitride/ PSG is deposited on the drain layer. After the multilayer stack is deposited, a rectangular vertical trench is etched through the entire stack. Then boron-doped crystalline silicon is grown by selective epitaxy to form P-type single-crystal device channel. The silicon channel is planarized using chemical mechanical polishing (CMP). After this the process is followed by forming source region by arsenic ion implantation, forming source-drain extension (SDEs) by solid source diffusion (SSD), depositing and etching nitride spacer and removing sacrificial gate layer. Finally gate oxide is grown, gate deposition and patterning is done.

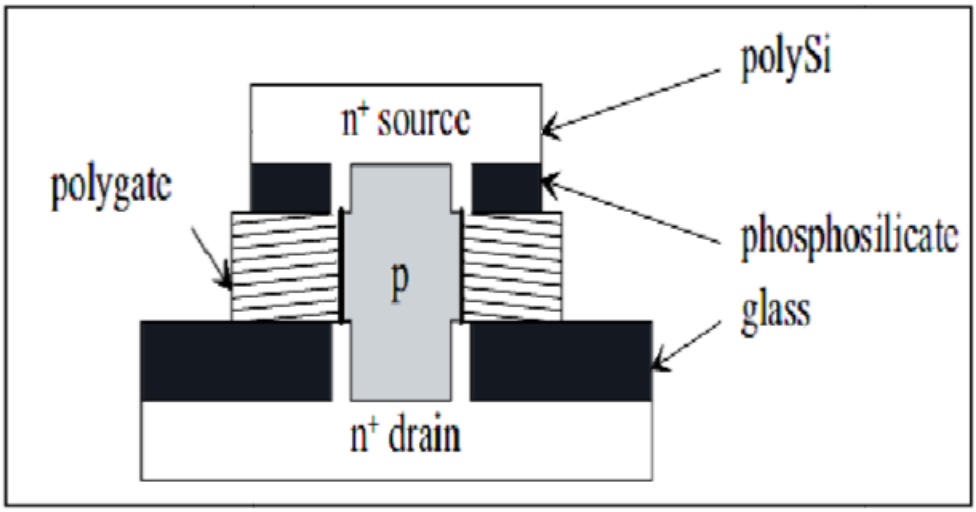

Figure 1-3:Vertical replacement gate MOSFET.

In this type of vertical MOSFETs, the overlap capacitances are much lower than the device, vertical MOSFETs based on epitaxy as it is determined by the thickness of the insulators between the PSG layers and the gate layer of this device. Because of source and drain extension across the entire width of the pillar, the parasitic bipolar transistor is found to be a problem. A partial solution is proposed by using a shallow polysilicon source pad to manufacture a leaky body contact [15]. Main disadvantage of this architecture is that it is not at all CMOS compatible due to the use of epitaxy.

1.2.3 Vertical MOSFETs based on ion implantation

Finally, the third type of vertical MOSFETs is the vertical MOSFETs based on ion-implantation [16-24] as illustrated in figure 1-4. The source and drain regions of this type of MOSFETs is formed by ion-implantation. The silicon pillar height and the implant energy determine the channel length of this type of MOSFETs.

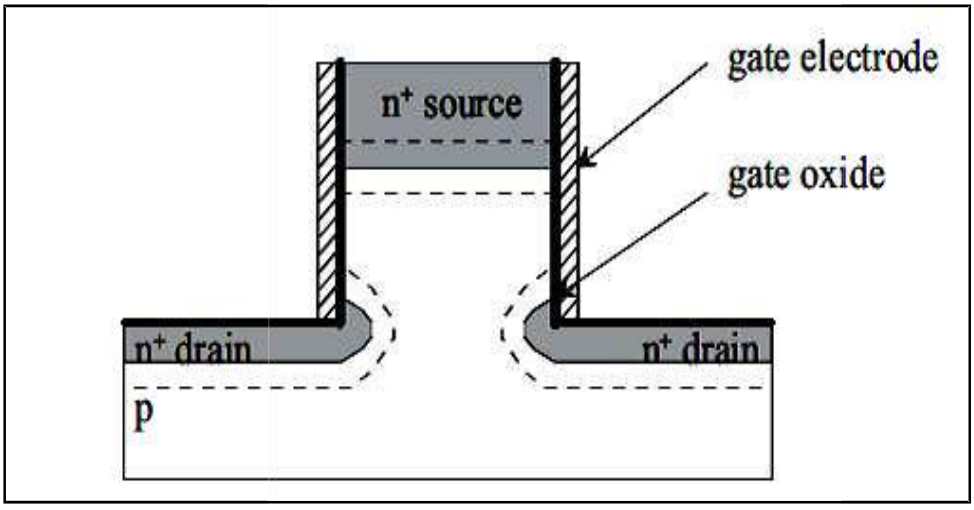

Figure 1-4:Vertical MOSFET based on ion implantation.

In this type of MOS device it is possible to give a narrow shape pillar with the gate surrounding the entire pillar and the channel is completely lithography independent. In this type of device the parasitic bipolar gain is lower than the device, vertical MOSFETs base on epitaxy. The main reason of that is the drain never penetrates across the width of the pillar. Another major advantage of this type device is CMOS compatibility while parasitic source/ drain overlap capacitance has been eliminated in this type of vertical MOSFETs devices using FILOX process [25] which made this type of devices most promising for industrial application. Filox process introduces thick oxide both at pillar top and bottom thereby ensuring gate overlap with source/drain region introduces low overlap capacitances. Extensive investigations have been done on this type of vertical MOSFETs [26, 27, 28] and recently this type of vertical MOSFET has been demonstrated as viable route for improving RF performance of matured CMOS technologies [26].

1.3 Thesis Objective:

In this thesis work we study the Process simulation of FILOX vertical MOSFET to estimate fabrication parameters for RF application. Different parameters are used to form 115nm channel length, 140nm Junction depth and 3.3nm gate oxide thickness for the fabrication of FILOX vertical MOSFET. This study would provide insight into choosing appropriate body doping and source/drain doping of 2×10^{20} cm^{-3}. To get the desired body doping we see the alteration of channel length 115nm and junction depth 140nm. Then we adjusted the dose and energy of FILOX vertical MOSFET.

1.4 Organization:

This thesis report is segmented into four different chapters. The first chapter describes the introduction of this thesis includes the motivation, vertical MOSFET and its background, objective and organization.

In second chapter, the simulation methodology is described elaborately. Here, we discuss the basic simulation technique of device simulation software ATHENA-SILVACO. The second chapter also describes the Simulation overview and simulation profile.

The third chapter describes the results elaborately including detail steps with figure of a FILOX Vertical MOSFET fabrication process. Finally, it shows figure of different desired body doping and source drain doping.

Lastly, in fourth chapter we describe the conclusion.

2 CHAPTER: SIMULATION METHODOLOGY

2.1 Simulation Overview

The device simulation is done using the commercial process simulator ATHENA - SILVACO. We describe of different desired body doping value for 115nm of channel length and 140nm of the junction depth, 3.3nm of gate oxide thickness and 2×10^{20} cm^{-3} of source/drain doping FILOX vertical MOSFET. The heavily doped drain and source region were formed using uniform doping concentration of 2×10^{20} cm^{-3} and the different desired body doping 4×10^{18} cm^{-3}, 2×10^{18} cm^{-3}, 1×10^{18} cm^{-3}, 8×10^{17} cm^{-3}, 6×10^{17} cm^{-3}, 4×10^{17} cm^{-3}, 2×10^{17} cm^{-3}, 1×10^{17} cm^{-3}, 8×10^{16} cm^{-3} and 6×10^{16} cm^{-3} were used for analysis of this device structure. Here the body was p-type and source drain and gate were n-type with uniform concentration.

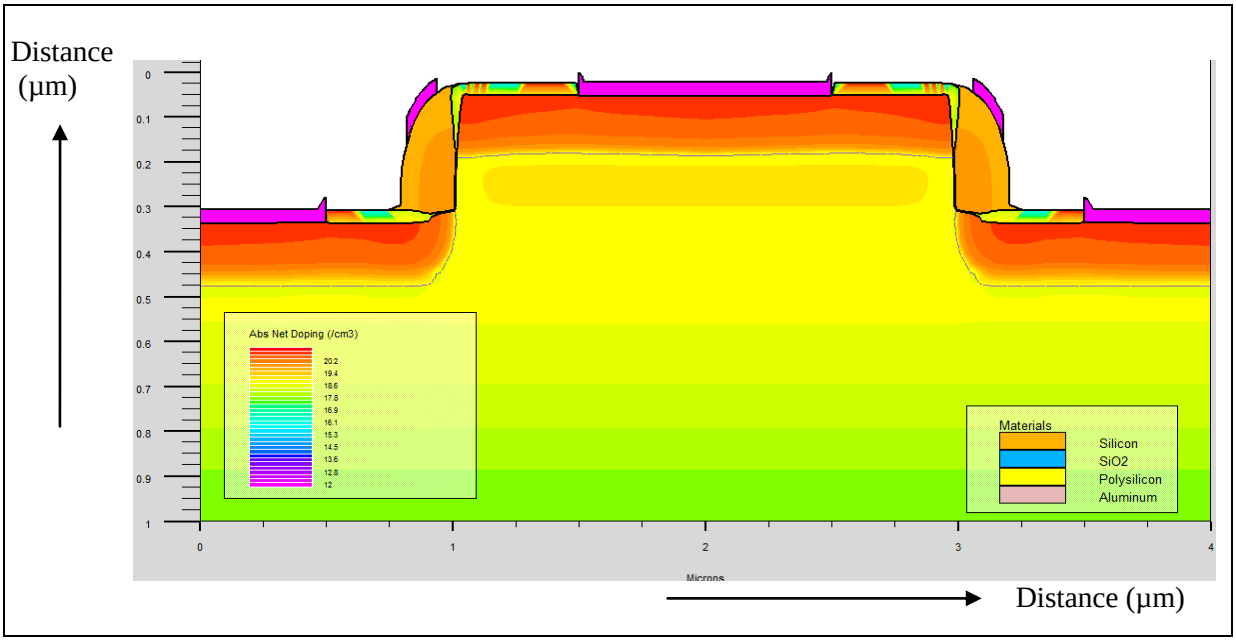

Figure 2-1: Schematic structure of FILOX vertical MOSFET.

To accurately create device grid structure, we ensured adequate mesh density in high field area such as channel region, source, drain and gate junction region. We have taken finer mesh at the interface of heavy doping and the light doping interface. We have removed grid lines from a specified device region where we expect a coarser grid using the ELIMINATE statement. A coarser grid is used at the substrate region in order to reduce

simulation run time and achieve more accuracy. The created device grid structure is shown below,

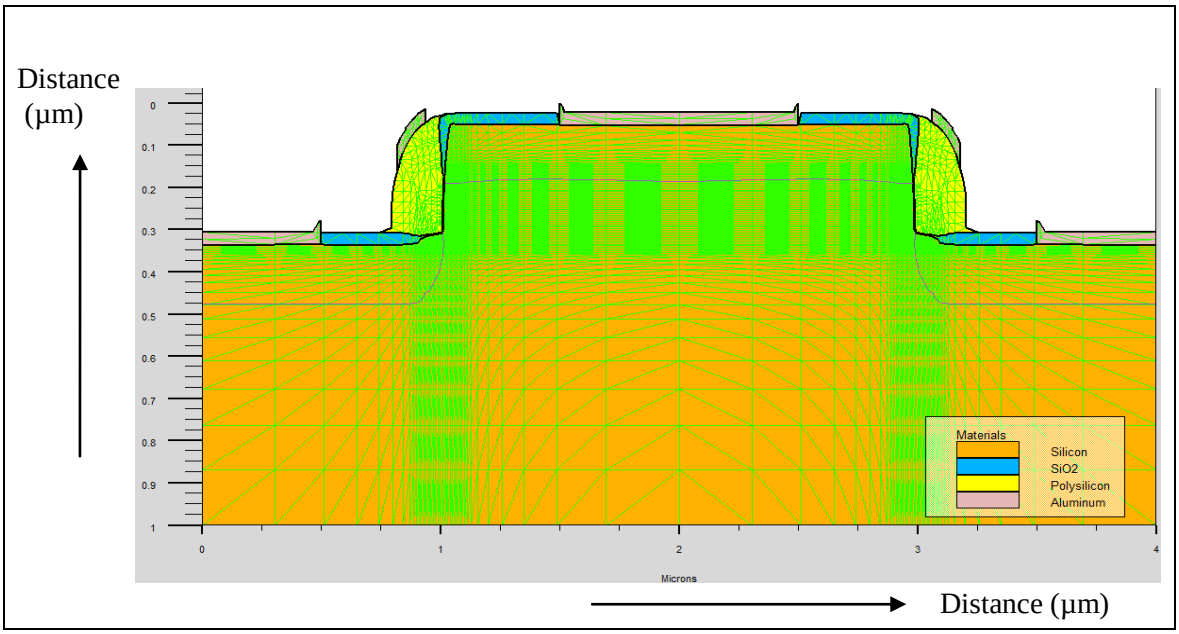

Figure 2-2: Cross-sectional view of FILOX vertical MOSFET for showing the grid density.

2.2 Simulation profile

Once the structure and the mesh were found to be as desired, the simulation was performed with appropriate models as discussed in section 2.1 and numerical solving methods. The model was invoked by using compress model, viscous model and Fermi model while keeping the accuracy of the simulation at an acceptable level.

2.2.1 The compress model

The compress model is activated by specifying compress in the method statement before the diffuse statement and default the oxidation model. It is also recommended for simulation the planar and the non-planar structure where the stress is playing a minor effect to determining the oxide shape. The Compress Model is activated by specifying COMPRESS in the METHOD statement prior to a DIFFUSE statement. The Compress Model is the default oxidation model in SSUPREM4 [29] .

Neglecting the acceleration and gravitational terms in the hydrodynamic flow equation, the creeping-flow equation is given by

$$\mu\nabla^2 \mathrm{V} = \nabla \mathrm{P} \qquad \textbf{(2.1)}$$

where P is the hydrostatic pressure, $\boldsymbol{V}$ is velocity of oxide elements and ∇ is the oxide viscosity.

The oxide viscosity is calculated from the following equation:

$$\mu = \frac{YOUNG.M}{(2 + 2\,.POISS.R)} \quad \textbf{(2.2)}$$

where *YOUNG.M* is Young's modulus, which is specified in the MATERIAL statement, and *POISS.R* is Poisson's ratio, which is specified in the MATERIAL statement.

The oxide flow is treated as an incompressible fluid. By doing this, it implies the density of the oxide is constant with respect to time. Applying this fact to the mass continuity equation, the incompressibility condition is given as

$$\nabla.V = 0 \quad \textbf{(2.3)}$$

The incompressibility condition in Equation (2.3) is implemented by allowing a slight compressibility of the flowing oxide. Thus, Equation (2.3) is modified to give the following equation:

$$\nabla.V = \frac{1 - (2\,.POISS.R)}{\mu} P \quad \textbf{(2.4)}$$

The solution of Equation (2.4) at each time step gives the velocity field of the flowing oxide elements. The Compress Model is recommended for simulations of planar and non-planar structures, where stress effects play a minor role in determining the oxide shape. When stress effects are important, you can use the Viscous oxidation model.

2.2.2 The viscous model

The viscous model is activated by specifying the viscous parameter in the method statement before the diffuse statement. This model calculates stress in the growing oxide and almost the same shape for the si/oxide as the dose compress model. This model is activated by specifying the VISCOUS parameter in the METHOD statement prior to the DIFFUSE statement. The Viscous Model calculates stresses in the growing oxide and creates almost the same shape for the silicon/oxide interface as does the Compress model [29]. The stresses in the oxide are calculated as follows:

$$\sigma_{xx} + \sigma_{yy} = \frac{2\,.VISC\,.0\,.\exp\left(\frac{-VISC\,.E}{kT}\right)}{1 - 2\,.\ POISS\,.R}\left(\frac{\partial v_x}{\partial x} + \frac{\partial v_y}{\partial y}\right) \quad \textbf{(2.5)}$$

$$\sigma_{xx} - \sigma_{yy} = 2 \cdot VISC.0 \cdot \exp\left(\frac{-VISC.E}{kT}\right)\left(\frac{\partial v_x}{\partial x} - \frac{\partial v_y}{\partial y}\right) \quad \textbf{(2.6)}$$

$$\sigma_{xy} = VISC.0 \cdot \exp\left(\frac{-VISC.E}{kT}\right)\left(\frac{\partial v_x}{\partial x} + \frac{\partial v_y}{\partial y}\right) \quad \textbf{(2.7)}$$

where v_x and v_y are the x and y components of flow velocity $\boldsymbol{v}$ respectively. VISC.0 and VISC.E are the pre-exponential and activation energy, respectively for viscosity, are specified on the MATERIAL statement.

The stress calculated by the Viscous oxidation model replace stress that may have been previously generated by the STRESS.HIST parameter in the STRESS statement.
The stress-dependent nonlinear model based on Eyring's work [29] allows a description of the real shape of LOCOS profiles with kinks on the interface. The model is turned on by specifying the STRESS.DEP parameter the OXIDE statement. Using Equation (2.1) and Equations (2.4–2.7), the non-linear solver first finds a linear solution for flow velocities and stresses and then uses the stresses obtained to calculate the reduction factors for oxidant diffusivity, D_{eff}, oxide viscosity, μ, and the interface reaction rate constant k as follows:

$$D^{(i)}eff = D^{(i-1)}eff \cdot \exp\left(\frac{V_d\left(\sigma_{xx} + \sigma_{yy}\right)}{kT}\right) \quad \textbf{(2.8)}$$

$$\mu^{(i)} - \mu^{(i-1)} \frac{\left(\frac{\tau V_c}{2kT}\right)}{\sin h\left(\frac{\tau V_c}{2kT}\right)} \quad \textbf{(2.9)}$$

$$k^{(i)} = k^{(i-1)} \cdot \exp\left(-\frac{\sigma_r V_r + \sigma_t V_t}{kT}\right) \quad \textbf{(2.10)}$$

where i is the iteration. V_d, V_c, V_r, and V_t are the activation volumes (in $Å^3$), specified in the OXIDE statement.
τ is the total shear stress:

$$\tau = \frac{1}{2}\sqrt{(\sigma_{xx} - \sigma_{yy})^2 + 4\sigma_{xy}^2} \quad \textbf{(2.11)}$$

σ_r is the normal component of the total stress:

$$\sigma_r = \sigma_{xx} n_x^2 + \sigma_{yy} n_y^2 + 2\sigma_{xy} n_x n_y \quad \textbf{(2.12)}$$

σ_t is the tangential component of the total stress:

$$\sigma_t = \sigma_{xx} n_y^2 + \sigma_{yy} n_x^2 + 2\sigma_{xy} n_x n_y \quad \textbf{(2.13)}$$

where n_x and n_y are the *x* and *y* components of the unit vector normal respectively. The reduced parameters feed back to the next iteration. This process continues until the accuracy criterion is met. Fast convergence of this process is not guaranteed. Oxidation calculations by the stress-dependent model usually take much more CPU time than the Compress Model.

2.2.3 The Fermi Model

The Fermi Model assumes that point defect populations are in thermodynamical equilibrium and thus need no direct representation. All effects of the point defects on dopant diffusion are built into the pair diffusivities. The main advantage for using the Fermi Diffusion model is it will greatly improve the simulation speed, since it does not directly represent point defects and only needs to simulate the diffusion of dopants. Also, the Fermi Model usually results in an easier numerical problem due to the avoidance of "numerical stiffness". But since point defects are not directly simulated, the Fermi model cannot deal with certain process conditions in which the defect populations are not in equilibrium, such as in wet oxidation (where Oxidation Enhanced Diffusion (OED) is important), emitter-base diffusions and wherever implantation results in an initial high level of implant damage.In the Fermi Model, each dopant obeys a continuity equation of the form:

$$D_{AX}\left(T.\frac{n}{n_i}\right) = D_{AX}^{x} + D_{AX}^{-}\left(\frac{n}{n_i}\right)^{1} + D_{AX}^{=}\left(\frac{n}{n_i}\right)^{2} + D_{AX}^{+}\left(\frac{n}{n_i}\right)^{-1} + D_{AX}^{++}\left(\frac{n}{n_i}\right)^{-2} \quad \textbf{(2.14)}$$

where C_{Ch} is the chemical impurity concentration, Z_A is the particle charge (+1 for donors and -1 for acceptors), D_{AV} and D_{AI} are the joint contributions to the dopant diffusivity from dopant-vacancy and dopant-interstitial pairs in different charge states. C_A is the mobile impurity concentration and *E* is the electric field.

The terms D_{AV} and D_{AI} depend on both the position of the Fermi level as well as temperature and are expressed as:

$$D_{AX}^{c} = D.0_{AX}^{c} \exp\left(-\frac{D.E_{AX}^{c}}{kT}\right) \quad \textbf{(2.15)}$$

where the temperature dependency is embedded in the intrinsic pair diffusivities, which are specified by Arrhenius expressions of the type:

$$\frac{\partial C_{Ch}}{\partial t} = \sum_{X=I,V} \nabla \cdot D_{AX}\left(\nabla C_A - Z_A C_A \frac{qE}{kT}\right) \quad \textbf{(2.16)}$$

Table 2-1 shows the names of the pre-exponential factors, *D.0*, and activation energies, *D.E*, for each of the charge states, *c*, of the various intrinsic pair diffusivity terms [29].
Pair charge states beyond two are unlikely to occur, which is why they have been omitted. Also, for most dopants it is seldom that more than three of the terms above are non-vanishing.

Table 2-1. Table of intrinsic pair diffusivities for different pair types

Pair	**Charge State**	**Pre--exponential factor**	**Activation Energy**
AV	X	DVX.0	DVX.E
AV	-	DVM.0	DVM.E
AV	=	DVMM.0	DVMM.E
AV	+	DVP.0	DVP.E
AV	++	DVPP.0	DVPP.E
AI	X	DIX.0	DIX.E

Pair	**Charge State**	**Pre--exponential factor**	**Activation Energy**
AI	-	DIM.0	DIM.E
AI	=	DIMM.0	DIMM.E
AI	+	DIP.0	DIP.E
AI	++	DIPP.0	DIPP.E

3 CHAPTER: RESULT

3.1 FILOX vertical MOSFET Fabrication Process

To create the vertical MOSFET structure we follow some instructions such as, A silicon wafer is taken as the starting material and a p-type body is formed by boron implantation having a boron dose of 5.0×10^{14} cm^{-2} and high-temperature drive-in with energy of 50 kev. Channel length is produced by varying the Si pillar with the help of dry etch, having a pillar height of 300nm. A sacrificial oxidation was performed to eliminate dry etch damage and reduce the surface roughness on the pillar sidewall. For the FILOX process a silicon nitride was deposited and anisotropically etched to create a nitride spacer. The nitride pacer is etched with the help of dry etch according to the desired shape. A FILOX oxide layer was thermally grown having a thickness of 60 nm. Arsenic implantation is performed then the source and drain are implanted. The nitride fillet and pad oxide are subsequently removed by wet etch afterward gate oxide is grown. A polysilicon gate is deposited and patterned by dry etch to create a surround gate. A rapid thermal annealing is done. Finally source and drain are patterned for metal contacts and aluminum contacts are formed. Final body doping was 4×10^{18} cm^{-3} and source/drain doping were 2×10^{20} cm^{-3}. FILOX vertical MOSFET fabrication steps are shown in the figures below,

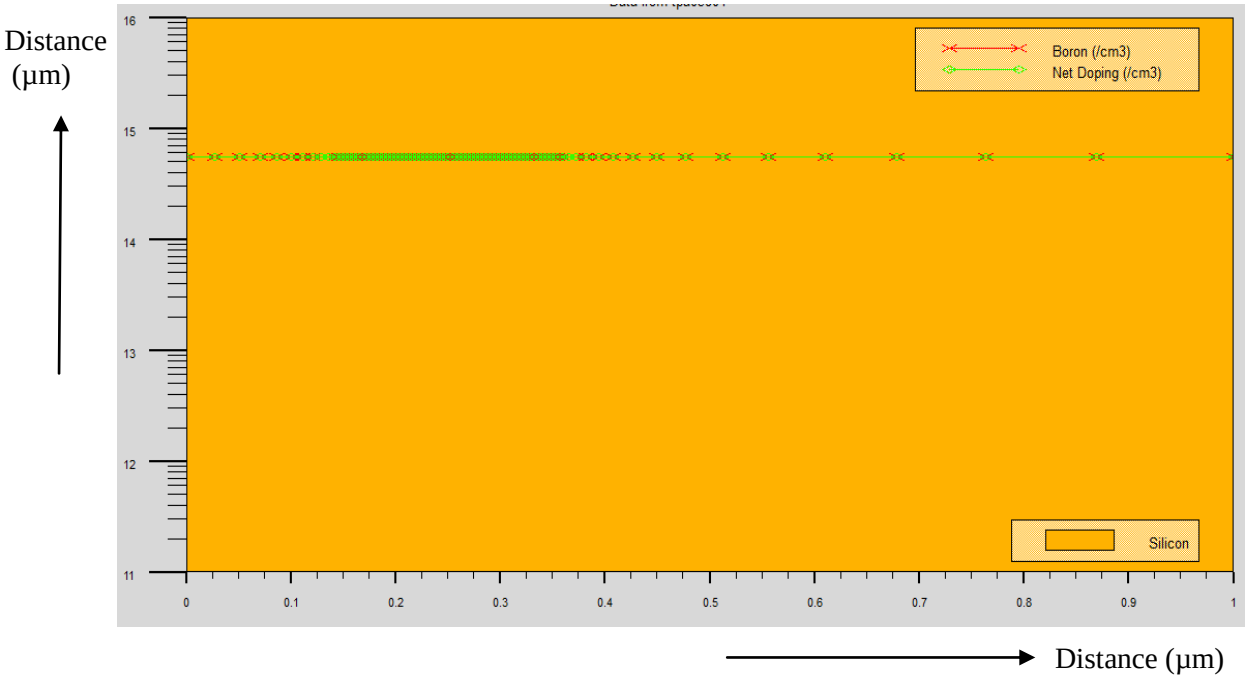

Figure 3-1: Net doping 5.0×10^{14} cm^{-3} of silicon wafer of FILOX vertical MOSFET.

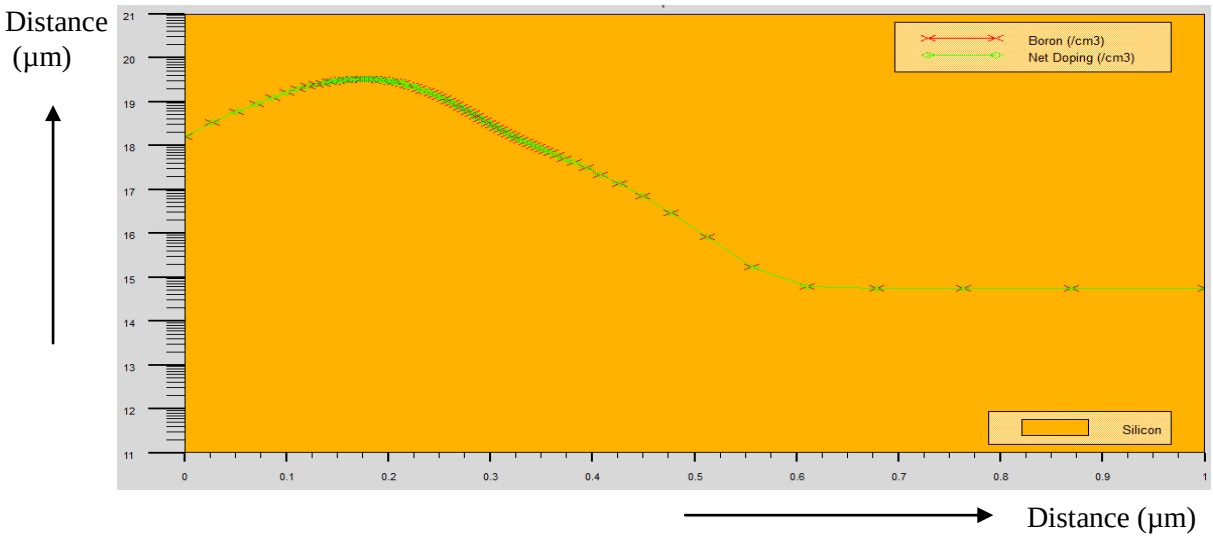

Figure 3-2: Net doping 1.0×10^{18} cm^{-3} by implanted with boron dose=5×10^{14} cm^{-2} of and energy=50 kev of silicon wafer of FILOX vertical MOSFET.

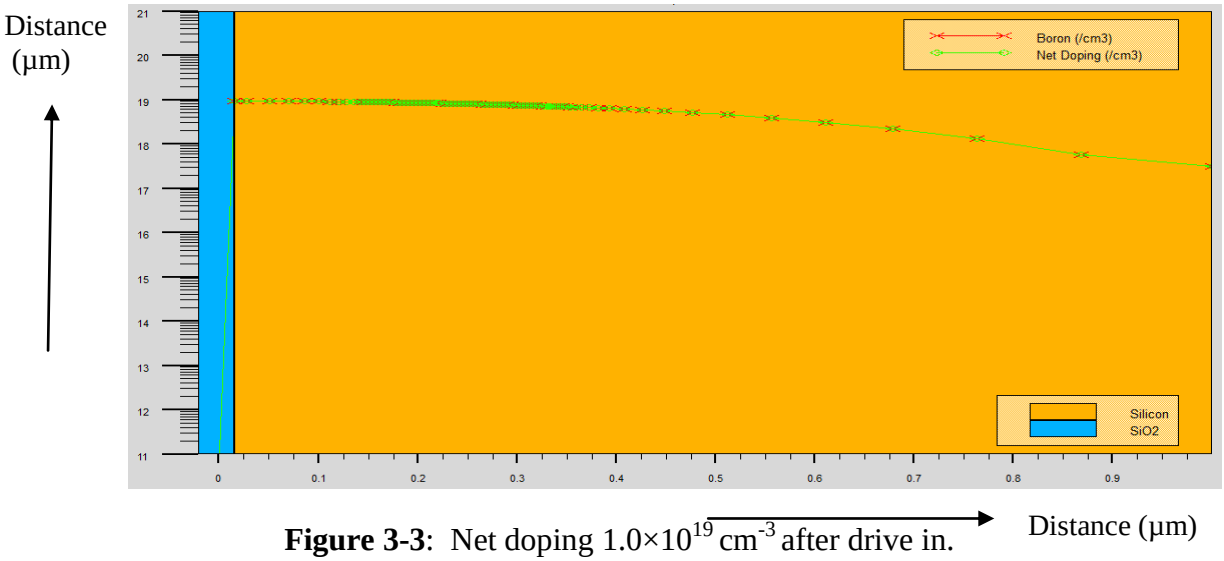

Figure 3-3: Net doping 1.0×10^{19} cm^{-3} after drive in.

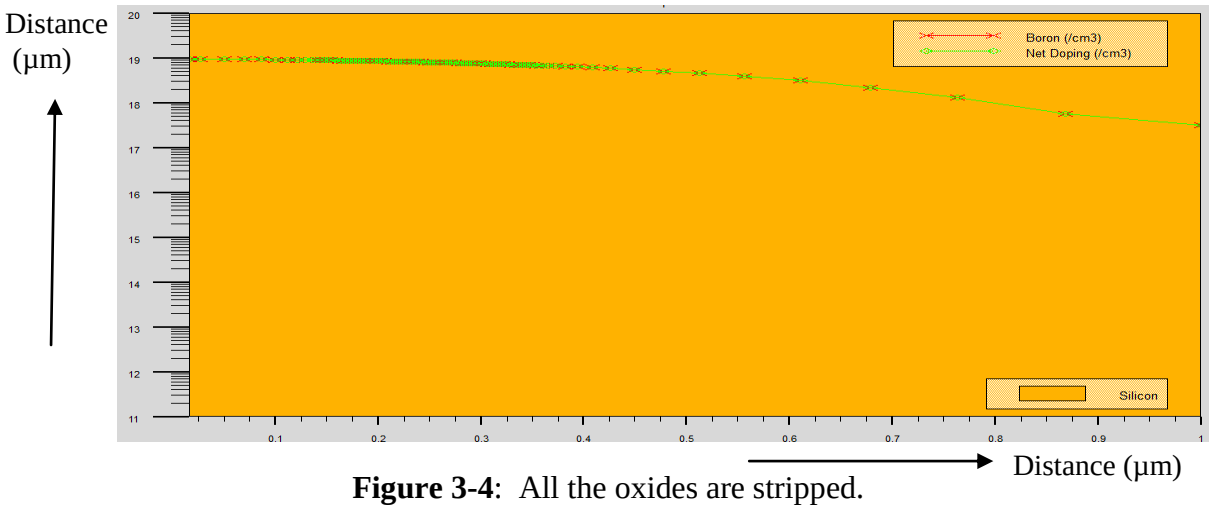

Figure 3-4: All the oxides are stripped.

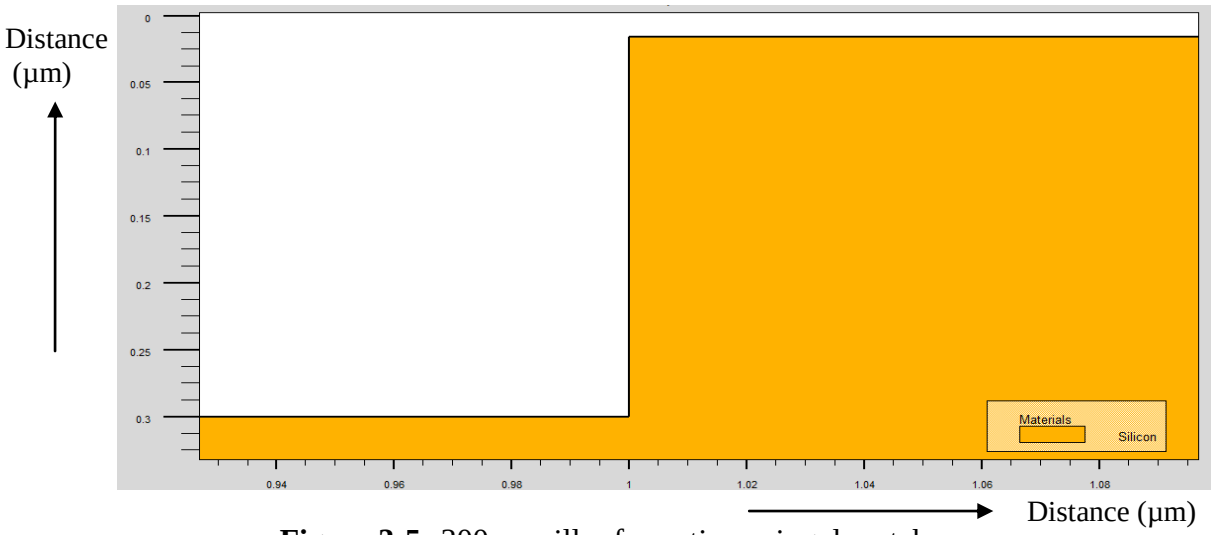

Figure 3-5: 300nm pillar formation using dry etch.

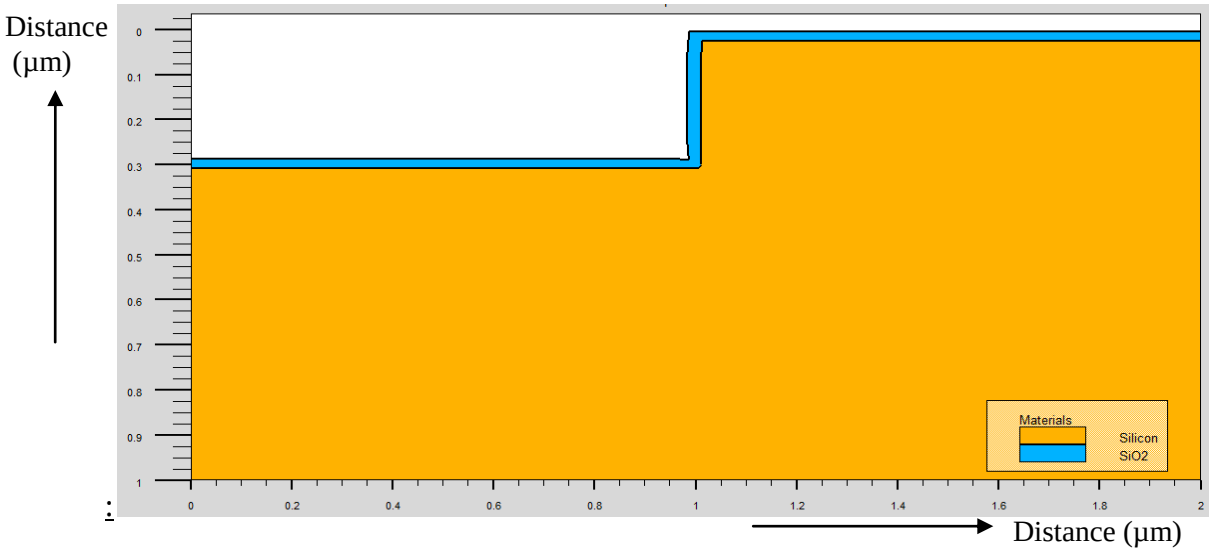

Figure 3-6: Deposition of pad oxide oxide=10 nm on the Pillar.

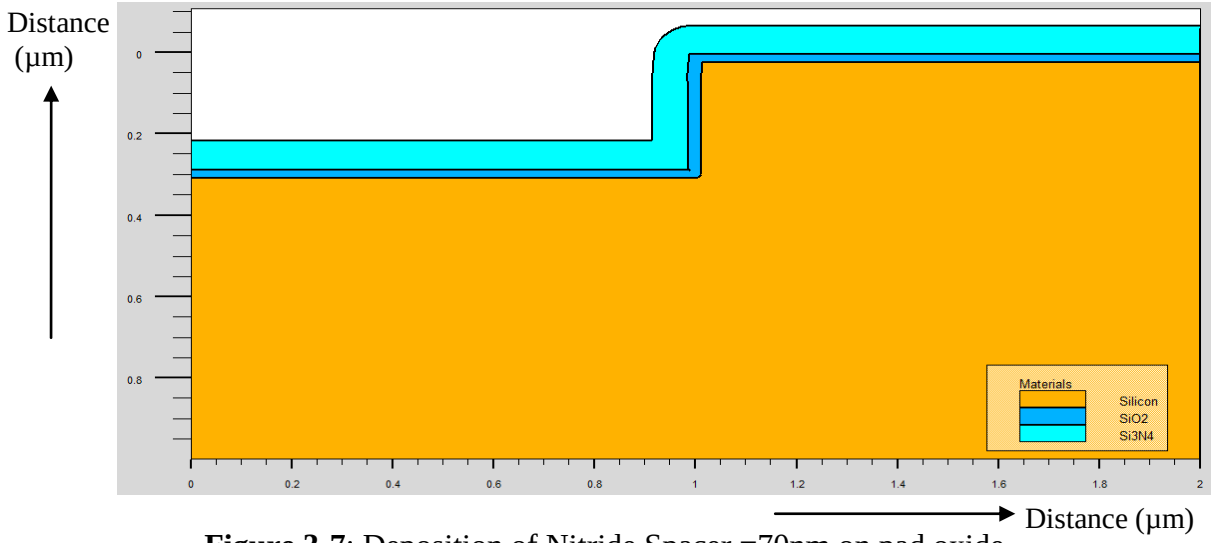

Figure 3-7: Deposition of Nitride Spacer =70nm on pad oxide.

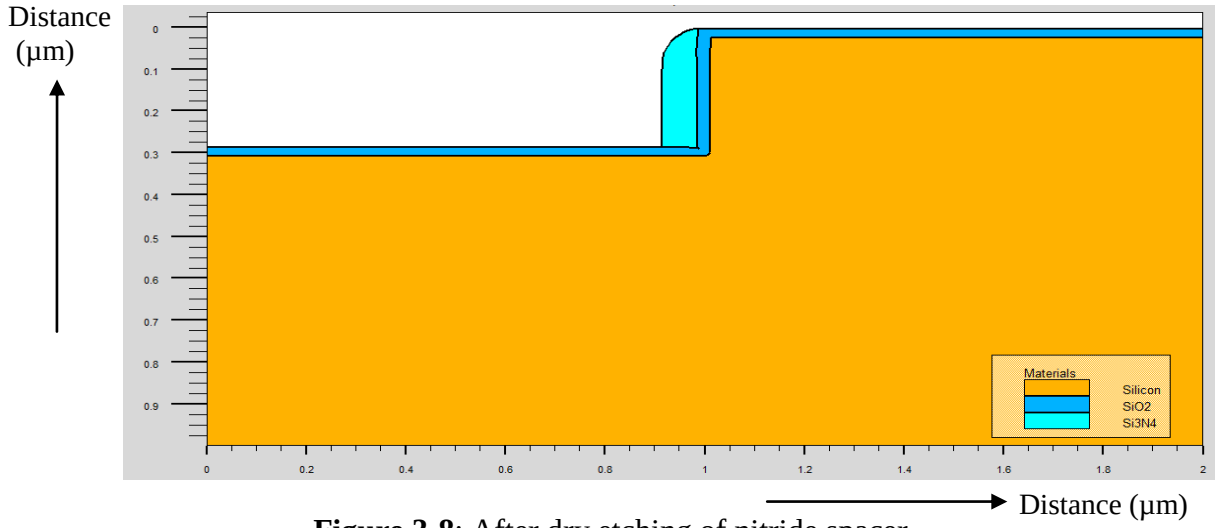

Figure 3-8: After dry etching of nitride spacer.

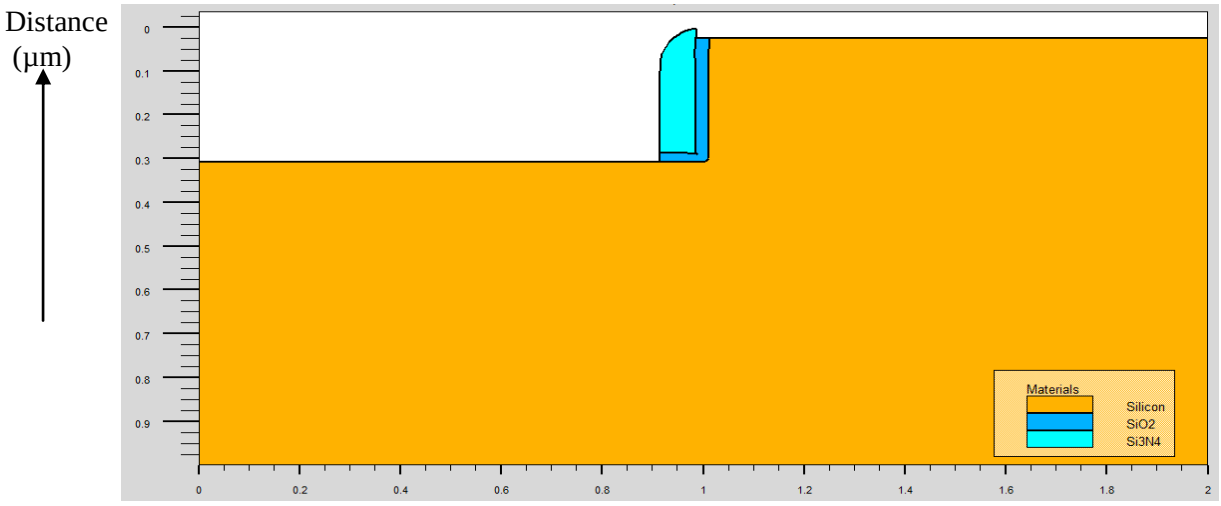

Figure 3-9: After etch of pad oxide.

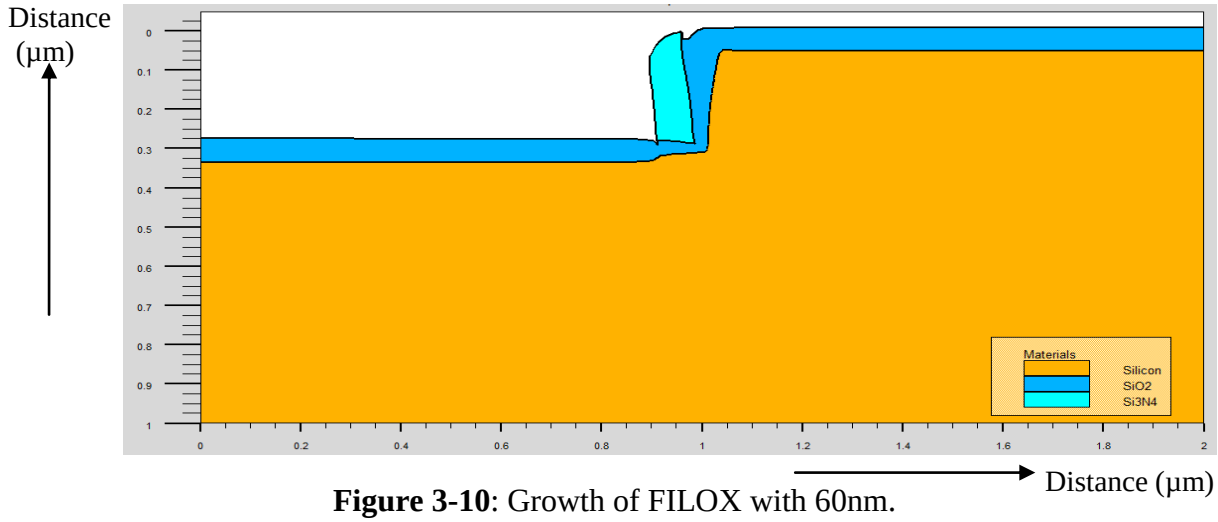

Figure 3-10: Growth of FILOX with 60nm.

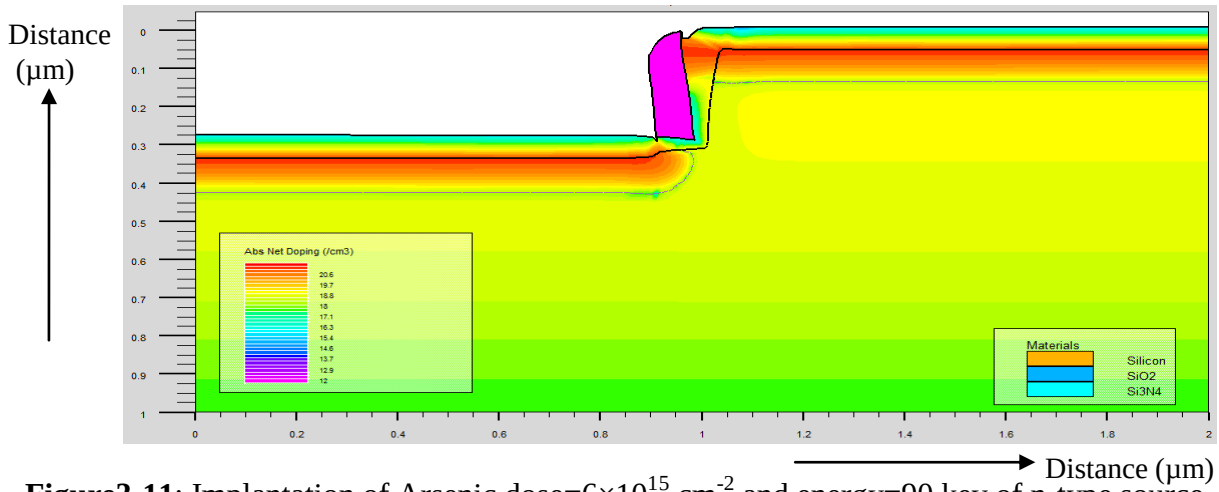

Figure3-11: Implantation of Arsenic dose=6×10^{15} cm^{-2} and energy=90 kev of n-type source and drain.

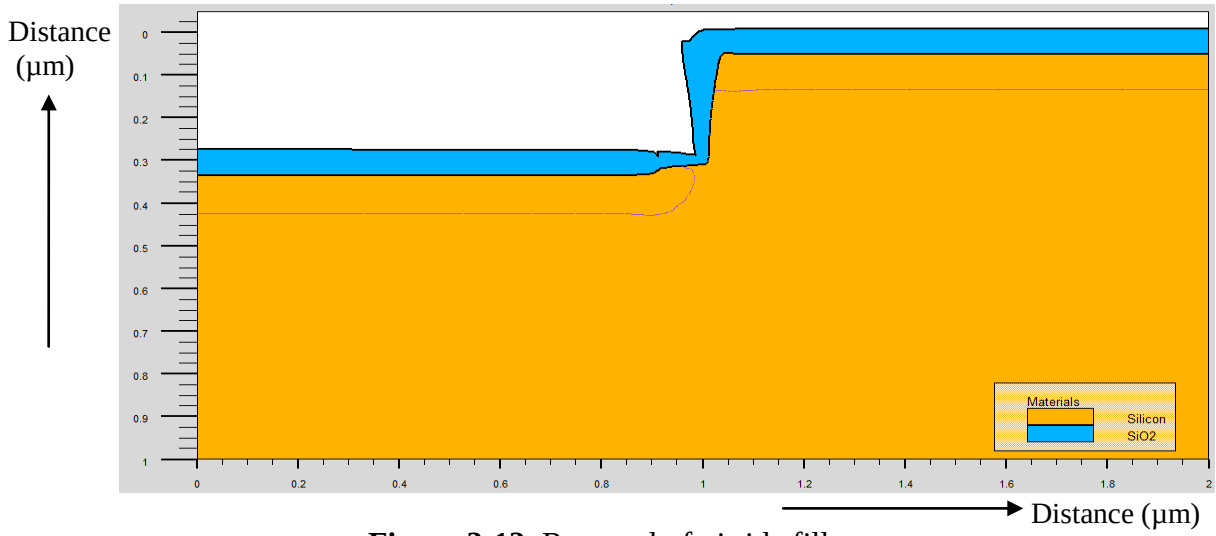

Figure 3-12: Removal of nitride fillet.

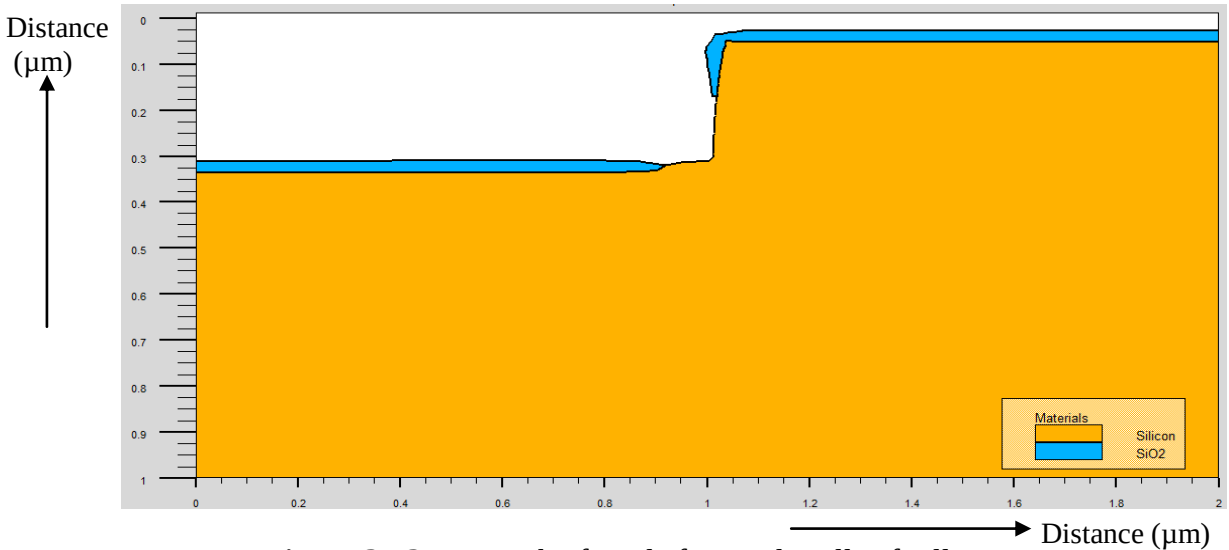

Figure 3-13: Wet etch of oxide from sidewalls of pillar.

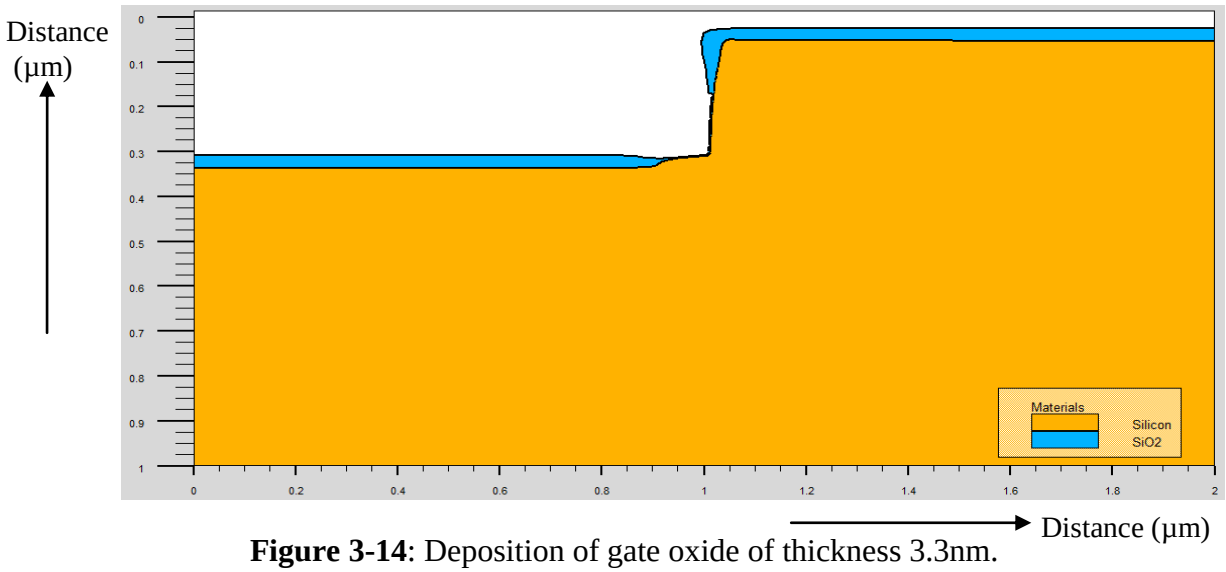

Figure 3-14: Deposition of gate oxide of thickness 3.3nm.

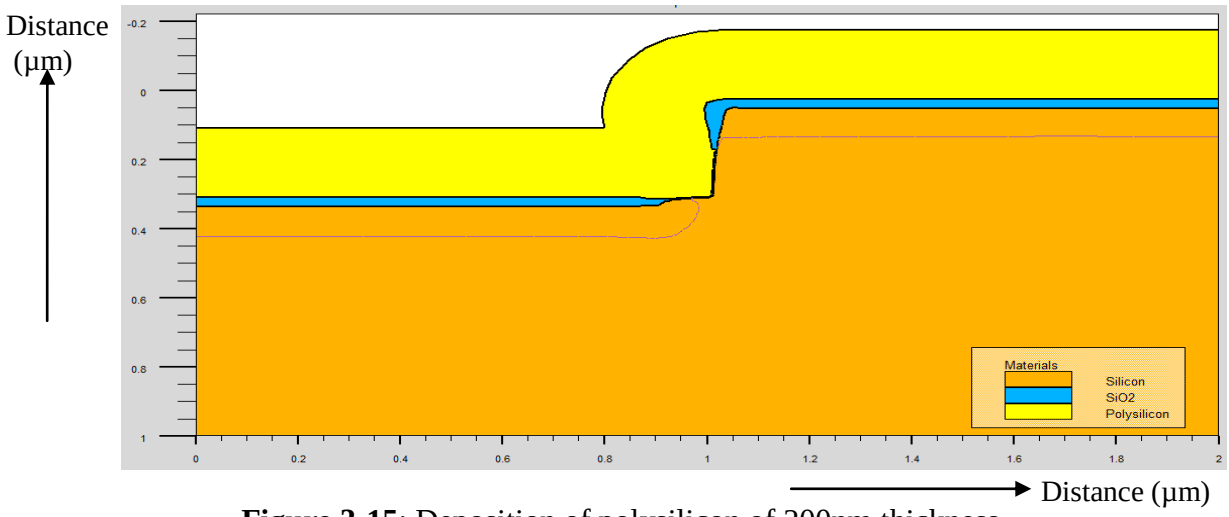

Figure 3-15: Deposition of polysilicon of 200nm thickness.

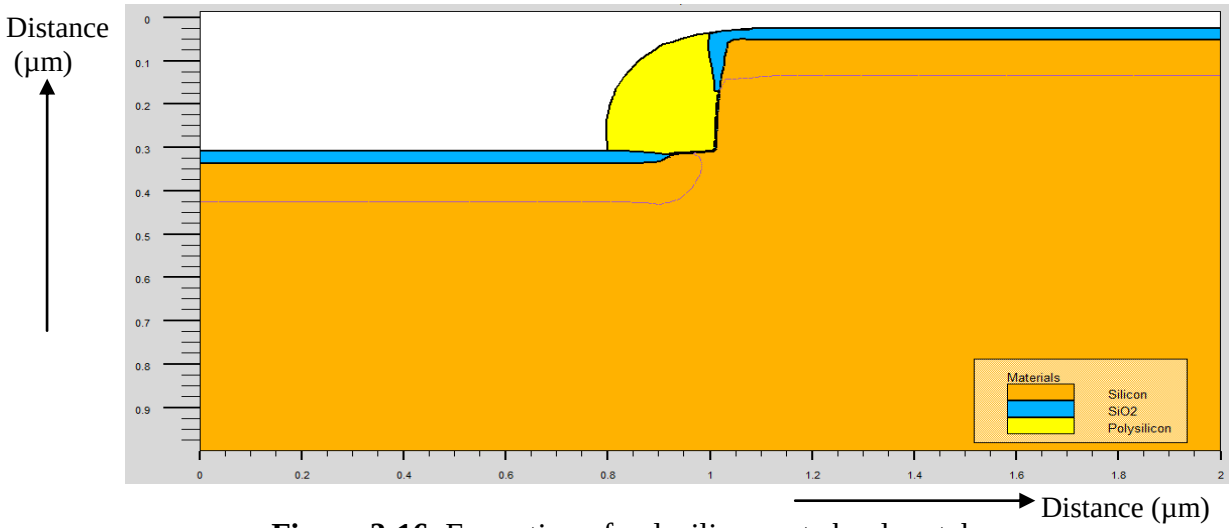

Figure 3-16: Formation of polysilicon gate by dry etch.

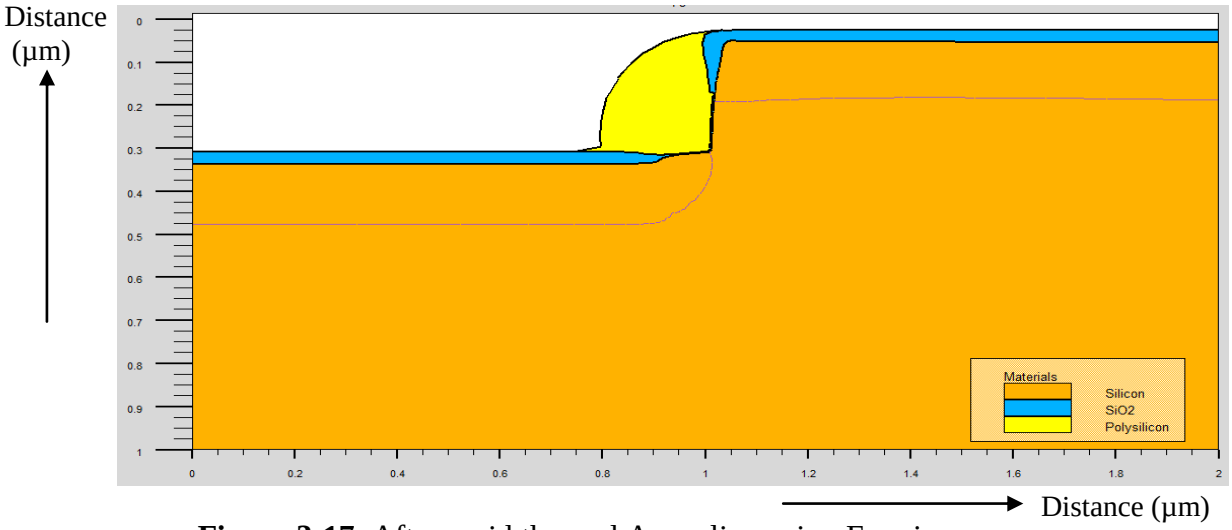

Figure 3-17: After rapid thermal Annealing using Fermi compress.

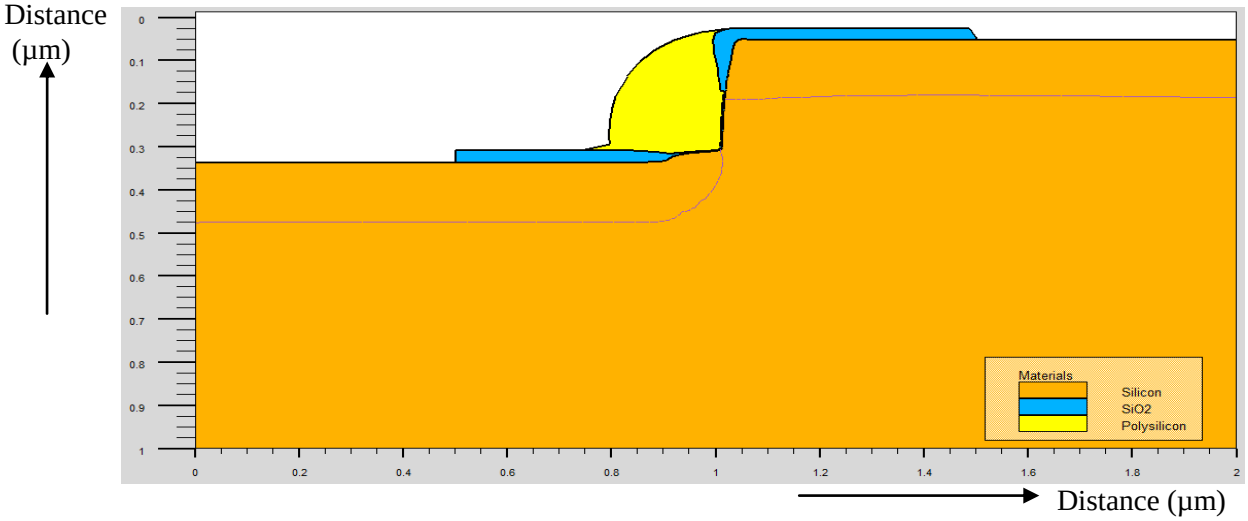

Figure 3-18: Pattern of source and drain for metal contact of FILOX vertical MOSFET.

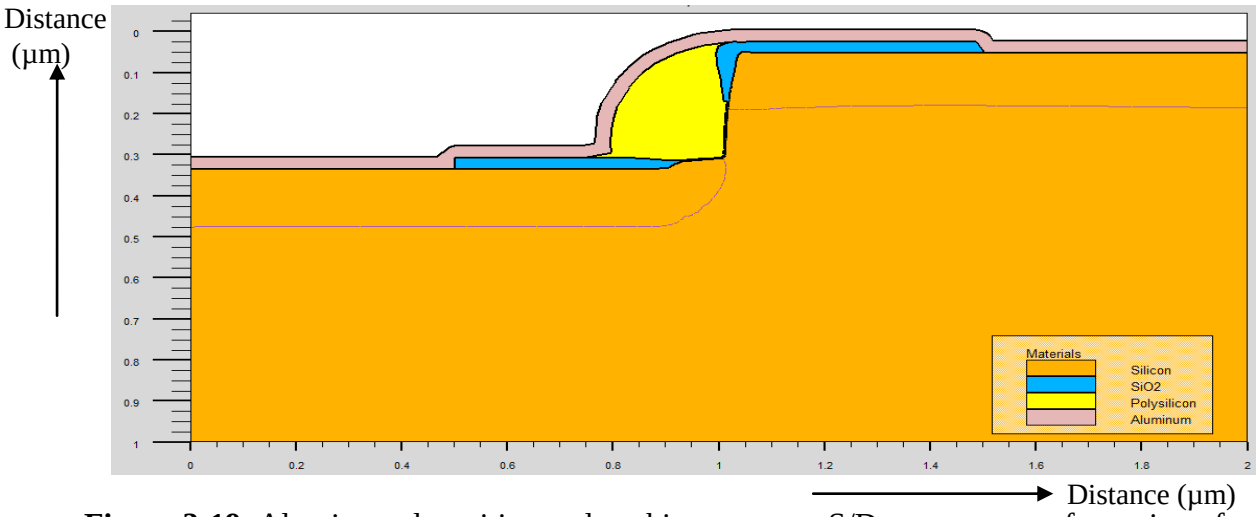

Figure 3-19: Aluminum deposition and etching to create S/D , gate contact formation of FILOX vertical MOSFET.

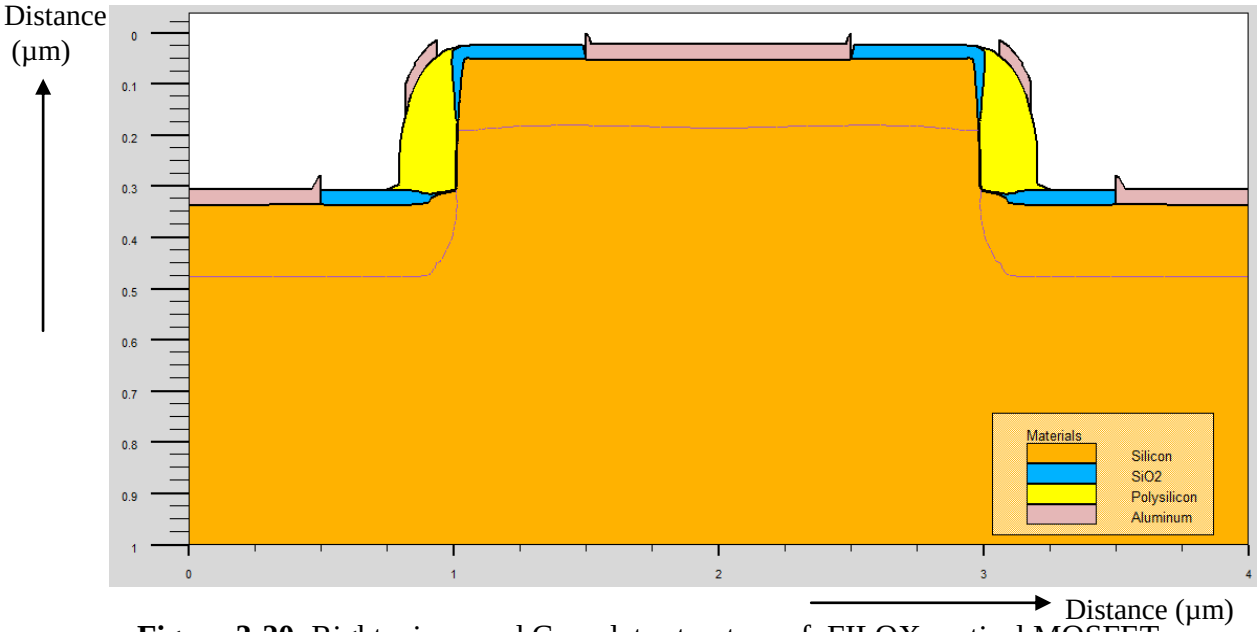

Figure 3-20: Right mirror and Complete structure of FILOX vertical MOSFET.

3.2 Process parameter for desired different Body and S/D doping values

This section describes figure of different desired body doping values for 115nm channel length, 140nm junction depth and 2×10^{20} cm^{-3} of source/drain doping of FILOX vertical MOSFET. For each body doping several random simulations required for adjusting dose anneal time. Change of body doping also changes S/D junction depth and hence we need to change S/D doping as well. Following figures show realized device doping profile from pillar top.

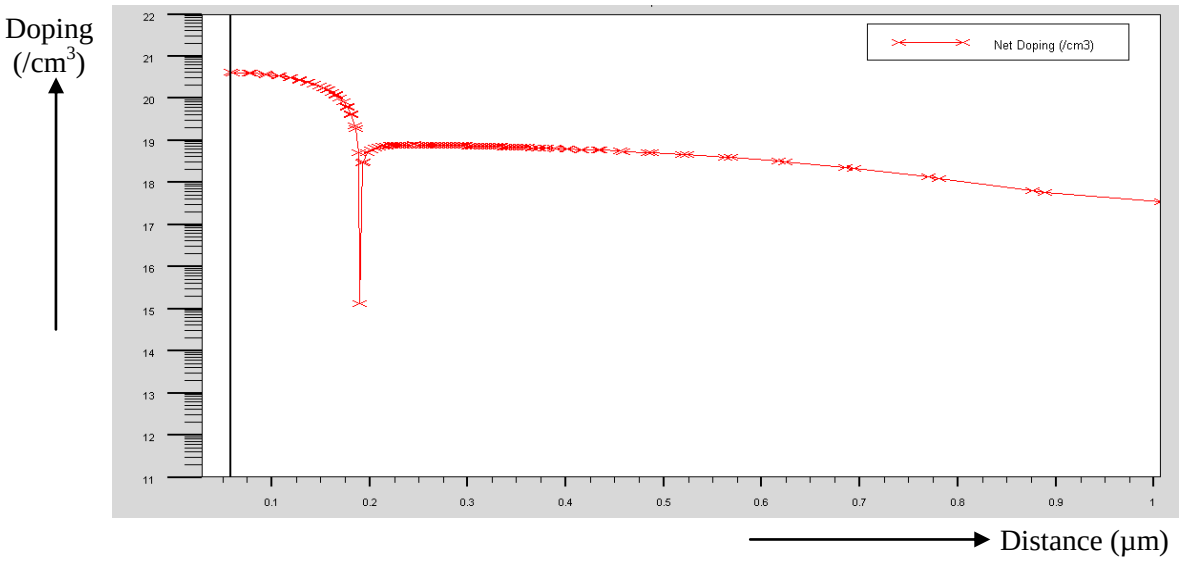

Figure 3-21:115 channel length FILOX vertical MOSFET with S/D doping 2×10^{20} cm^{-3} and net body doping of 4×10^{18} cm^{-3}.

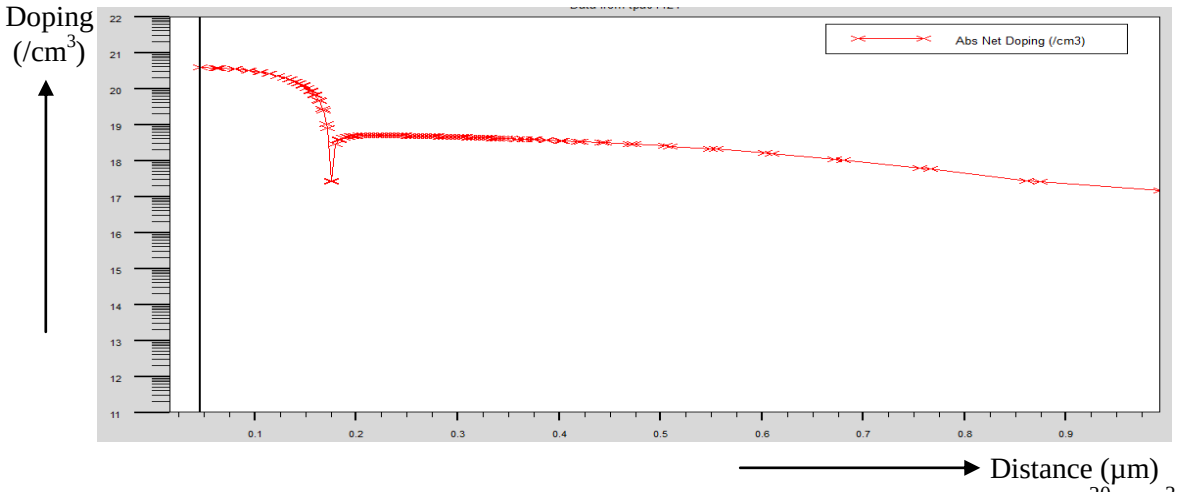

Figure 3-22: 115 channel length FILOX vertical MOSFET with S/D doping 2×10^{20} cm^{-3} and net body doping of 2×10^{18} cm^{-3}.

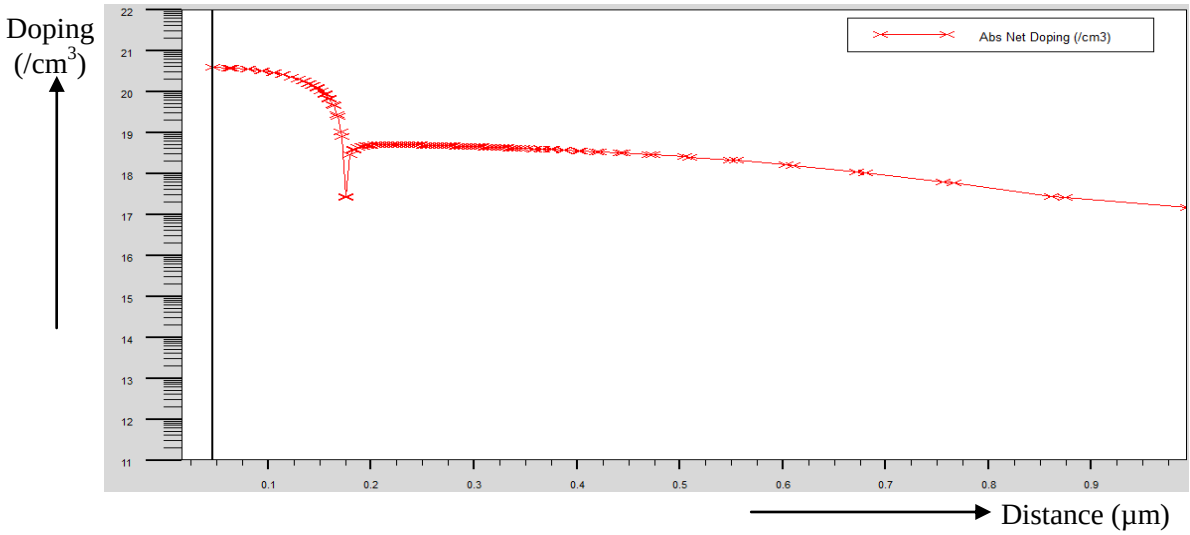

Figure 3-23:115 channel length FILOX vertical MOSFET with S/D doping 2×10^{20} cm^{-3} and net body doping of $1\times10^{18}$$cm^{-3}$.

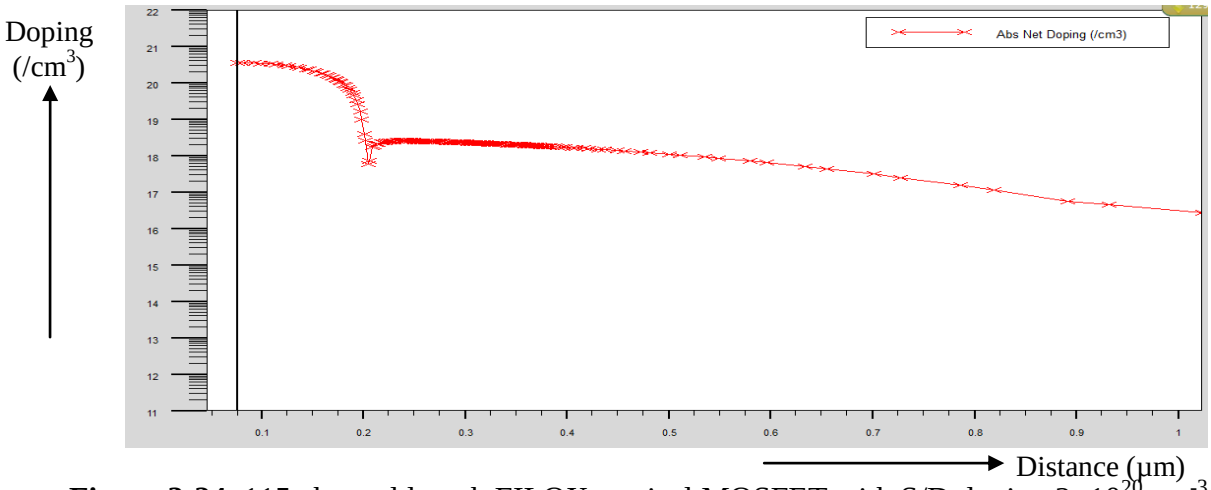

Figure 3-24: 115 channel length FILOX vertical MOSFET with S/D doping 2×10^{20} cm^{-3} and net body doping of 8×10^{17} cm^{-3}.

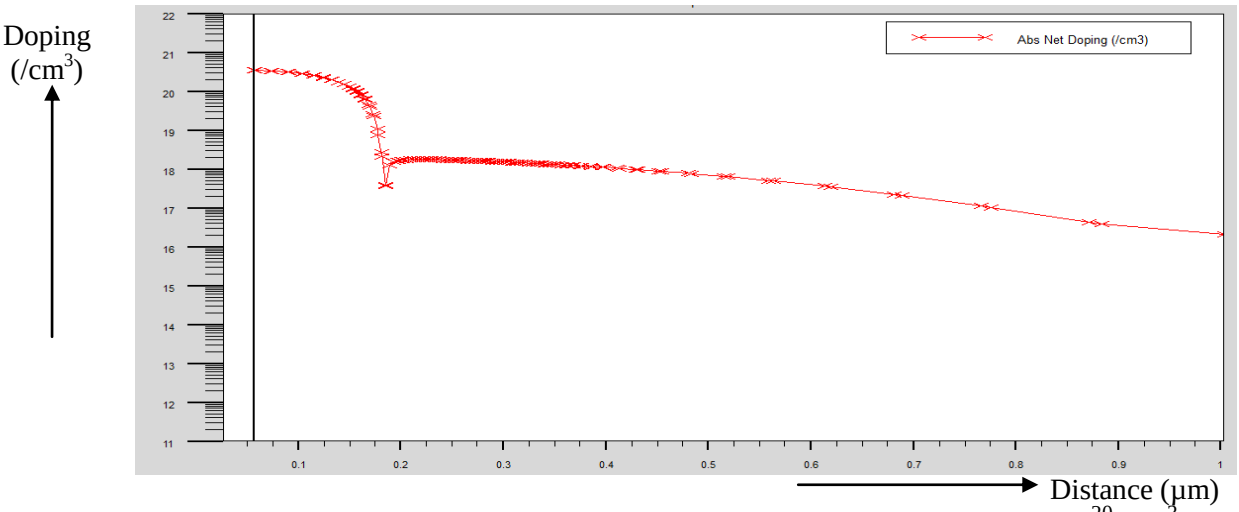

Figure 3-25: 115 channel length FILOX vertical MOSFET with S/D doping 2×10^{20} cm^{-3} and net body doping of 6×10^{17} cm^{-3}.

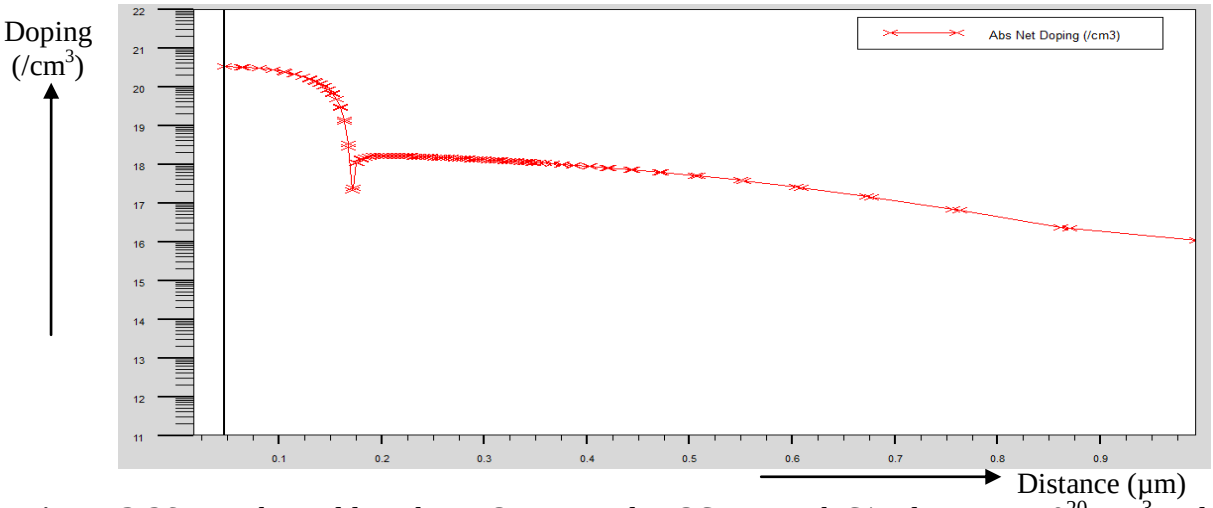

Figure 3-26:115 channel length FILOX vertical MOSFET with S/D doping 2×10^{20} cm^{-3} and net body doping of 4×10^{17} cm^{-3}.

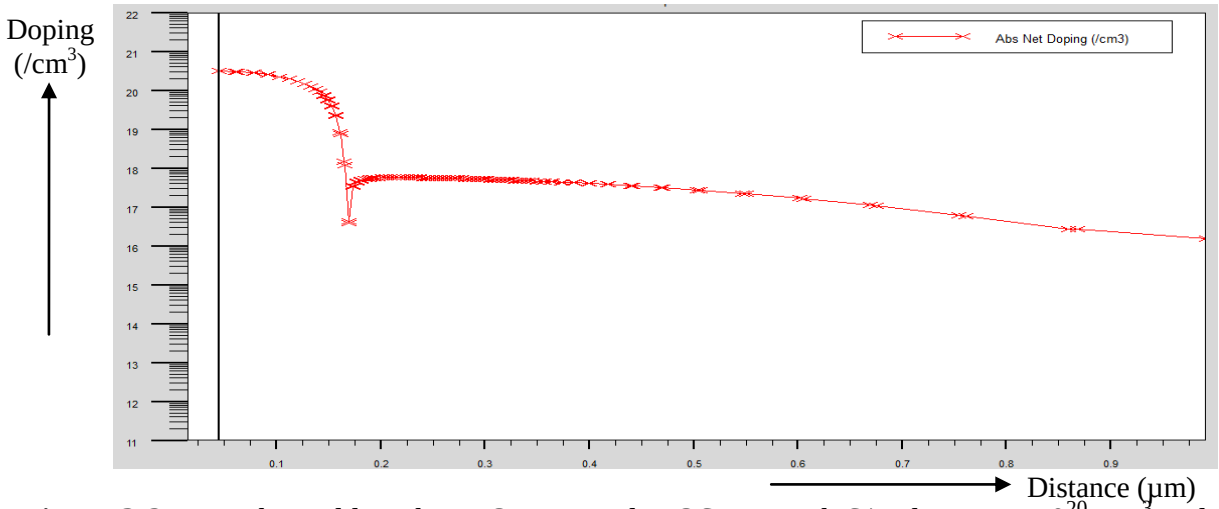

Figure 3-27:115 channel length FILOX vertical MOSFET with S/D doping 2×10^{20} cm^{-3} and net body doping of 2×10^{17} cm^{-3}.

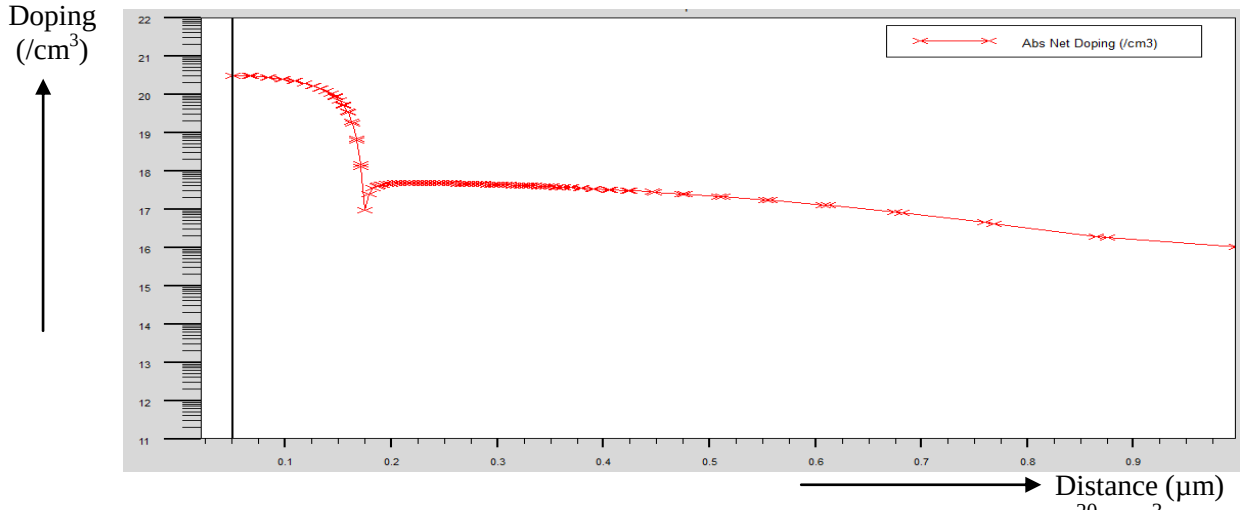

Figure 3-28:115 channel length FILOX vertical MOSFET with S/D doping 2×10^{20} cm^{-3} and net body doping of 1×10^{17} cm^{-3}.

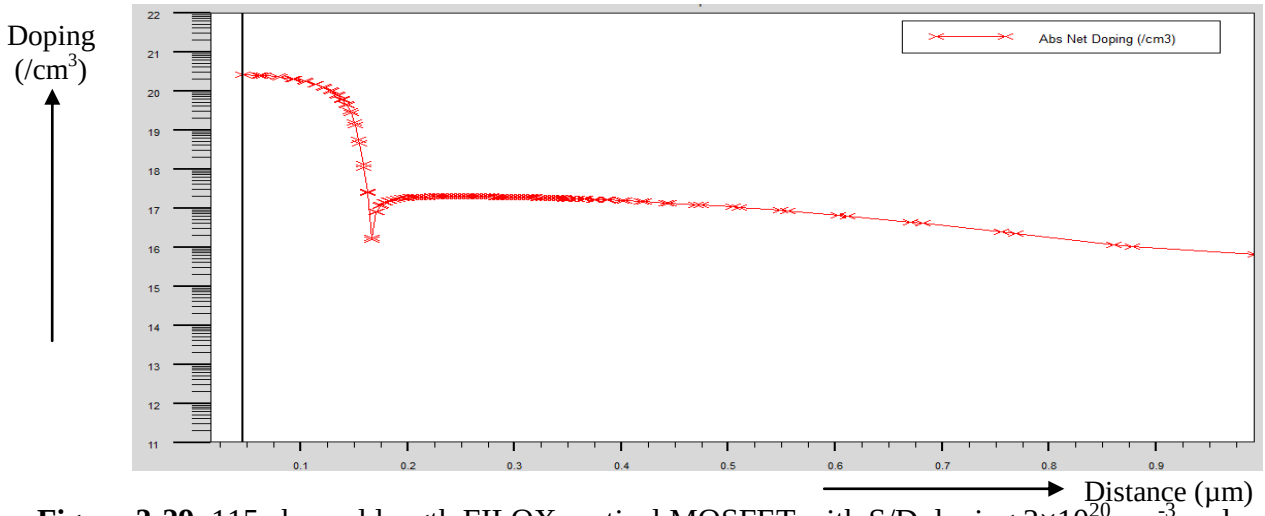

Figure 3-29: 115 channel length FILOX vertical MOSFET with S/D doping 2×10^{20} cm^{-3} and net body doping of 8×10^{16} cm^{-3}.

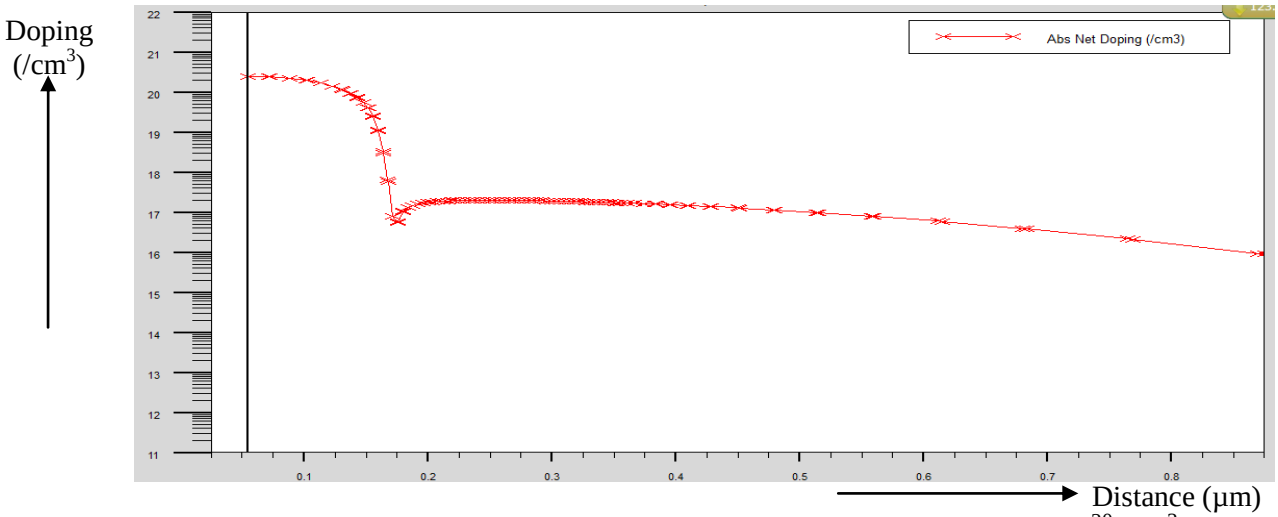

Figure 3-30: 115 channel length FILOX vertical MOSFET with S/D doping 2×10^{20} cm^{-3} and net body doping of 6×10^{16} cm^{-3}.

4 CHAPTER

4.1 CONCLUSION

In this thesis, we observe process simulation of FILOX vertical MOSFET to estimate fabrication parameters. A simple self-aligned process has been developed to reduce the parasitic overlap capacitance in vertical MOSFETs using nitride spacers on the sidewalls of the trench or pillar and a local oxidation. We describe different step of FILOX vertical MOSFET Fabrication and finally we get 115nm of channel length, 140nm of the junction depth, gate 3.3nm of oxide thickness, 4×10^{18} cm^{-3} of body doping and 2×10^{20} cm^{-3} of source/drain doping in the FILOX vertical MOSFET. To get the desired body doping we see the alteration of channel length 115nm and junction depth 140nm. Then we adjusted the dose and energy of FILOX vertical MOSFET.

4.2 Table

This section describes result of desired body doping value for 115nm of channel length and 140nm of the junction depth and 2×10^{20} cm^{-3} of source/drain doping FILOX vertical MOSFET. We observe desired body doping below in the table,

Table 4-1 for p-type implant:

	Dose (cm^{-2})	Energy (kev)	Channel length(nm)	Doping(Body) (cm^{-3})
i.	5.0×10^{14}	50	115	4×10^{18}
ii.	3.0×10^{14}	45	115	2×10^{18}
iii.	2.0×10^{14}	30	115	1×10^{18}
iv.	1.4×10^{14}	27	115	8×10^{17}
v.	1.0×10^{14}	26	115	6×10^{17}
vi.	0.9×10^{14}	13	115	4×10^{17}
vii.	3.6×10^{13}	52	115	2×10^{17}
viii.	3.0×10^{13}	44	115	1×10^{17}
ix.	1.4×10^{13}	55	115	8×10^{16}
x.	1.4×10^{13}	48	115	6×10^{16}

Table 4-2 for n-type implant:

	Dose (cm^{-2})	Energy (kev)	Junction depth(nm)	Doping(S/D) (cm^{-3})
i.	6.0×10^{15}	90	140	2×10^{20}
ii.	6.0×10^{15}	85	140	2×10^{20}
iii.	6.0×10^{15}	84	140	2×10^{20}
iv.	6.0×10^{15}	82	140	2×10^{20}
v.	6.0×10^{15}	80	140	2×10^{20}
vi.	6.0×10^{15}	78	140	2×10^{20}
vii.	6.0×10^{15}	76	140	2×10^{20}
viii.	5.6×10^{15}	76	140	2×10^{20}
ix.	5.5×10^{15}	70	140	2×10^{20}
x.	5.5×10^{15}	69	140	2×10^{20}

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