DESIGN, CONSTRUCTION AND ANALYSIS OF A SINGLE PHASE INVERTER

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ABSTRACT

A single phase inverter is designed and constructed to provide regulated output voltage at 220V. The output power stage is designed in two methods first one is using four power transformers in H-bridge mode to the load through a transformer, and another one is two NMOS power transistors coupled to the load through a transformer. The output is a 50Hz square wave which is obtained by totem-pole driver operation of two transistors using 50 Hz complementary trigger pulse stream for first method. And for the second method 50Hz square wave is obtained using a single PNP transistor. The inverter is constructed and presented. The circuit is tested and it is found that the waveforms obtained at different stages of the circuit conform well to those obtained by computer simulation. The inverter circuit is found to be efficient for applications in appliances.

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APPROVAL

The project titled **'Design, construction and analysis of a single phase inverter'** submitted by M. Saddam Hossain Khan (2007-2-80-011), Mashfiqul Islam (2007-2-80-012) and Md. Ishanatur Rahman (2007-2-80-015), has been accepted as satisfactory in partial fulfillment of the requirements for the degree of Bachelor in Science in Electrical and Electronic Engineering on April 2011.

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AUTHORIZATION

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CHAPTER 1
INTRODUCTION

1.1 Introduction

Utilities supply ac voltage at fixed voltage and frequency. However, there are many applications where variable voltage and frequency are required. Inverter is equipment that converts input dc voltage to variable frequency and variable amplitude ac voltage. One of the important application of inverter is variable speed ac drives, where input ac is made variable (frequency and amplitude) by rectifier-inverter configuration.

The output voltage waveforms of ideal inverter should be sinusoidal and contain certain harmonics. For low and medium power applications, square wave or quasi square wave voltage may be acceptable; and for high power applications, low distorted sinusoidal waveforms are required.

In most inverter applications, it is necessary to be able to control both the output voltage and the output frequency. The controllable voltage requirement may arise out of the need to overcome regulation in the connected ac equipment or to maintain constant flux in ac motors driven at variable speed by variation of their supply frequency. If the dc input voltage is controllable, then an inverter with a fixed ratio of dc input voltage may be satisfactory. If the dc input voltage is not controllable, then the control of output voltage must be obtained by employing pulse width modulation.

Some applications of inverters are:

- Stand-by power supplies.
- Induction heating.
- Variable ac motor drives.
- Uninterruptable power supplies for computers.
- Aircraft power supplies.
- Output of dc transmission lines.
- Air conditioning.

Different types of Inverter

- Single phase inverter
- Three phase inverter
- Poly phase inverter
- High voltage inverter
- Multi-level inverter

...ording to source:

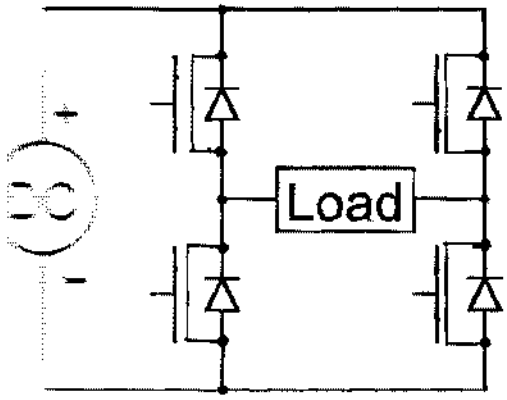
- Voltage source inverter
- Current source inverter

The Proposed Method

...le phase square wave is used as switching function to operate the proposed single ... inverter. Transistors are used as switches. The triggering of these switching devices is ... ed from two complement square waves and by a feedback loop from output to the ... This produces closed loop control which maintains constant output voltage under ... load conditions.

...ware implementation, we are proposing two methods.

...od 1. the proposed inverter is an H-Bridge type where two N type MOSFETs and two ... MOSFETs are used. The NMOS are used for negative switching and the PMOS are ... positive switching which enables more efficiency and lesser voltage drop in the ... Ts during switching.



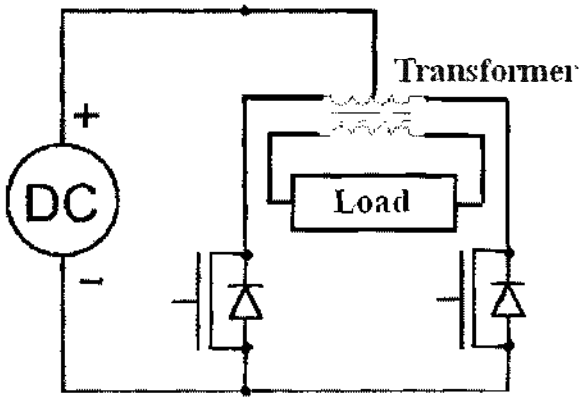


Fig 1.3.1 Block Diagram for Method 1

Fig 1.3.2 Block Diagram for Method 2

... 2. the proposed inverter is basically a push-pull arrangement which is a full bridge ... where the negative switching is done using two N type MOSFETs and the positive ... connected directly to the transformer at the load. This enables to minimize the power ... as there is no switching involved in the positive side.

... pose of using these two methods is to fulfill our target of achieving maximum ... at the output.

Scope of the Project

... load. it is difficult to keep the output voltage constant. The scope and objective of this ... is to maintain the constant output voltage at different loads and also to increase the ... of the inverter i.e. get the maximum voltage at the output node with minimum loss ... switching.

1.5 Introduction to the Chapters

The contents of this project have been organized as follows:

In chapter 2, the principle of operation of a single phase half bridge inverter and a full bridge inverter is discussed. The modulation technique used and the computer simulated outputs of the proposed inverter are shown n discussed in this chapter as well.

The design, construction and analysis of the proposed inverter are discussed in Chapter 3. The functional description of the two methods used, the PWM square wave generation using SG3524 and all the other devices and parts used in the construction is individually discussed in this chapter. The details of design, construction and testing are also discussed.

The technique of improving the efficiency of the proposed inverter and the analysis of the efficiency is discussed in Chapter 4.

Chapter 5 presents the conclusion, summary of the whole paper and the future improvements possible for the proposed inverter.

CHAPTER 2
PRINCIPLE OF OPERATION AND COMPUTER SIMULATION FOR PROPOSED METHOD

2.1 Introduction

In this chapter the principle of operation of a single-phase inverter is discussed. Both half and full bridge inverter with mathematical analysis are discussed. Fourier series is used for mathematical analysis. The input current of a single-phase inverter is also analyzed.

2.2 Principle of Operation

The operations of single phase half and full bridge inverters are discussed in the following sub-sections:

2.2.1 Operation of a Single Phase Half Bridge Inverter

The principle operation of a single-phase half bridge inverter can be explained with the help of the given figure. The inverter consists of two choppers. When only transistor Q_1 is turned on for a time $T_0/2$, the instantaneous voltage across the load v_0 is $V_S/2$. If only transistor Q_2 is turned on for a time $T_0/2$, $-V_S/2$ appears across the load. The logic circuit has to be designed such a way that Q_1 & Q_2 are not turned on at simultaneously. Figure 2.2.b shows the waveforms for the output voltage and transistor currents with the resistive load. This inverter requires three-wire dc source, and when transistor Q_2 is off, its reverse voltage instead of $V_S/2$. This inverter is known as a half wave bridge inverter.

... square (rms) output voltage can be found from

$$\frac{2}{T_0}\int_0^{T_0/2}\frac{V_s^2}{4}\,dt = V_S/2 \quad \ldots\ldots\ldots \text{(i)}$$

... instantaneous voltage can be expressed in Fourier series as

$$v_o = \sum_{n=1,3,5}^{\infty}(a_n\cos(n\omega t) + b_n\sin(n\omega t)) \quad \ldots\ldots\ldots \text{(ii)}$$

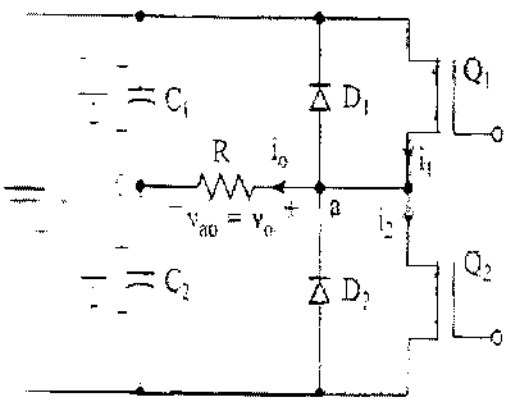
... quarter-wave symmetry along the x-axis, both a_0 and a_n are zero. We get b_n as

$$\frac{2}{T_0}\left[\int_0^{\pi}\frac{V_s}{2}\,d(\omega t) + \int_0^{\pi/2}\frac{V_s}{2}\,d(\omega t)\right] = \frac{4V_s}{n\pi} \quad \ldots\ldots\ldots \text{(iii)}$$

... the instantaneous output voltage Vo as

$$v_o = \sum_{n=1,3,5}^{\infty}\frac{2V_s}{n\pi}\sin(n\omega t)) \quad \ldots\ldots\ldots \text{(iv)}$$

... n=2,4,6 .....



... Block Diagram of Half Bridge

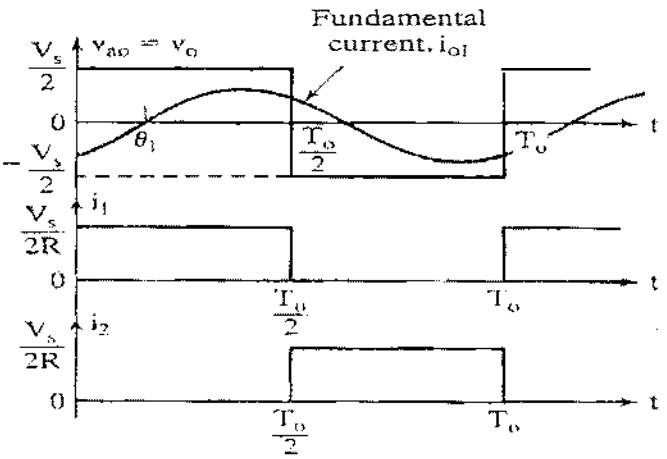
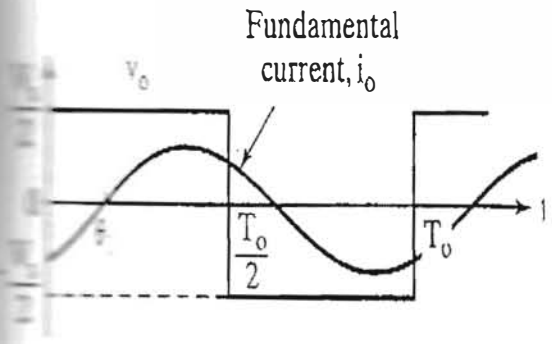


Fig: 2.2.1(b) Voltage Waveform

... current cannot change immediately with output voltage for an inductive load. When ... off at T0/2, the load current begins to flow through D2 and the lower half of the ... until the current falls to zero. Similarly when Q2 turned off at T0 the load current ... through D1 and the upper half of the DC source until the current falls to zero. ... are called feedback diodes. Energy is fed back to the DC source when these two ...



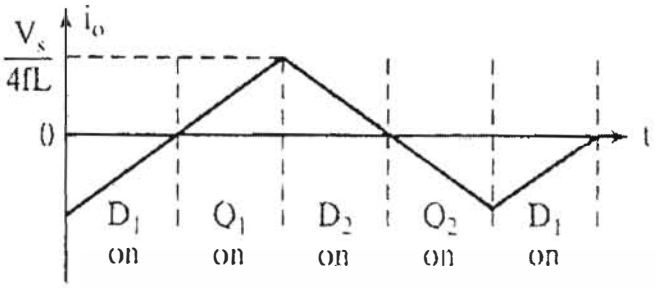


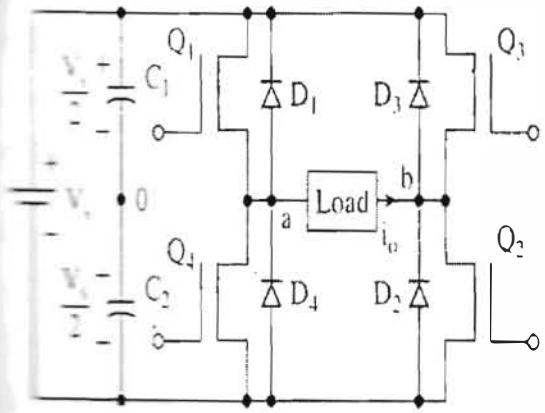
Fig 2.1.1(c) Voltage waveform

Fig 2.1.1(d) Current Waveform

For purely inductive load each of the transistors conducts only for T0/2. Depending upon the load impedance of a conduction period of a transistor can vary from 90°-180°.

2.3 Operation of a Single Phase full Bridge Inverter

The principle operation of a single-phase full bridge inverter can be explained with the help of figure 2.1a. A single-phase full bridge inverter consists of 4 choppers Q1 Q2 Q3 & Q4. While Q1 & Q2 turns on together, the output voltage remains Vs. If Q3 and Q4 turn on simultaneously –Vs appears at the output of the inverter. The logic circuit has to be designed such a way that Q1, Q2 or Q3, Q4 are not turned on at a same time. The output current waveform for highly inductive load is shown in following figure.



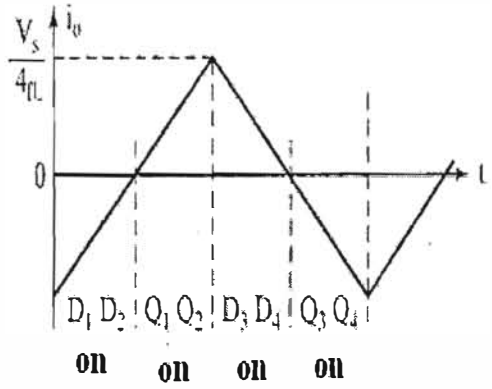


Fig 2.3(a) Block Diagram of Full Bridge

Fig 2.3(b) Current Waveform

The rms output can be found from

$$V_{rms} = \left(\frac{2}{T_0}\int_0^{To/2}\frac{V_s^2}{4}\,dt\right)^{1/2} = Vs \ldots\ldots\ldots (v)$$

The instantaneous voltage can be expressed in Fourier series as

$$V_0 = \sum_{n=1,3,5\ldots} \frac{4Vs}{n\pi} \sin(n\omega t) \ldots\ldots\ldots \text{(vi)}$$

The following table shows the switching states for full bridge inverter

State	State No	Switch State	Va0	Vb0	V0	Component Conducting
S1 and S2 are ON and S4 and S3 are OFF	1	10	Vs/2	-Vs/2	Vs	S1 and S2 if i0>0 D1 and D2 if i0<0.
S4 and S3 are ON and S1 and S2 are OFF	2	01	-Vs/2	Vs/2	-Vs	D4 and D3 if i0>0. S4 and S3 if i0<0
S1 and S3 are ON and S4 and S2 are OFF	3	11	Vs/2	Vs/2	0	S1 and D3 if i0>0. D1 and S3 if i0<0
S4 and S2 are ON and S1 and S3 are OFF	4	00	-Vs/2	-Vs/2	0	D4 and S2 if i0>0. S4 and D2 if i0<0
S4 and S2 are ON and S1 and S3 are OFF	5	OFF	-Vs/2 Vs/2	-Vs/2 -Vs/2	-Vs Vs	D4 and D3 if i0>0. D1 and D2 if i0<0

Table 2.2.2(a) Switching states of Full Bridge Inverter

The controllable transistor sign Q is replaced with S.

Modulation Technique

[illegible] in simple terms, is the process of changing multiple properties of a high-frequency [illegible] waveform (the carrier signal) with respect to a modulating signal. There are three key [illegible] of a periodic waveform- amplitude, phase and frequency. All of these parameters can be [illegible] with a low frequency signal in order to obtain the modulated signal. In most of the cases, the [illegible] signal is a high-frequency sinusoid waveform. However, a square wave pulse train is also a [illegible] come [13].

[illegible] inverter gain can be varied following multiple techniques the most efficient method of which is to [illegible] gain and output voltage and to incorporate pulse width modulation (PWM) control within [illegible]. Pulse-width modulation (PWM) is used to control power which is then used as input to [illegible] electrical devices. Turning the switch between supply and load on and off at a fast pace [illegible] the average value of voltage (and current) fed to the load, and this would not have been [illegible] without the help of modern switches. The time length for which the switch is left on is [illegible] as the magnitude of the power supply to the load. The PWM switching frequency has to be [illegible] faster to have an effect on the device that uses the power. Observations suggest switching have [illegible] several times a minute in an electric stove, 120 Hz in a lamp dimmer, from few kilohertz [illegible] tens of kHz for a motor drive and well into the tens or hundreds of kHz in audio amplifiers [illegible] computer power supplies[14].

[illegible] main advantages of PWM is that it brings down the power loss in the switching devices. In [illegible] off mode, it barely allows any flow of current and there is almost no voltage drop across the [illegible] when it is on. This signifies that the power loss in insignificant as it results from the product of [illegible] and current, both of which has near zero values in both on and off states. PWM is more than [illegible] with digital controls because they can easily set the needed duty cycle (duty cycle being [illegible] ratio of 'on' time to the regular interval or 'period' of time); low power succeeds a low duty [illegible]

[illegible] is required for another reason. That is for the adjustment of pulse width. Short [illegible] effect of a leg for an inverter can be avoided. If duty cycle remains 50% for both of the [illegible] inverter leg may burn, due to short circuit. It is known that MOSFET takes a [illegible] time to switch ON or switch OFF. So a minimum interval period requires, which is [illegible] existing duty cycle.

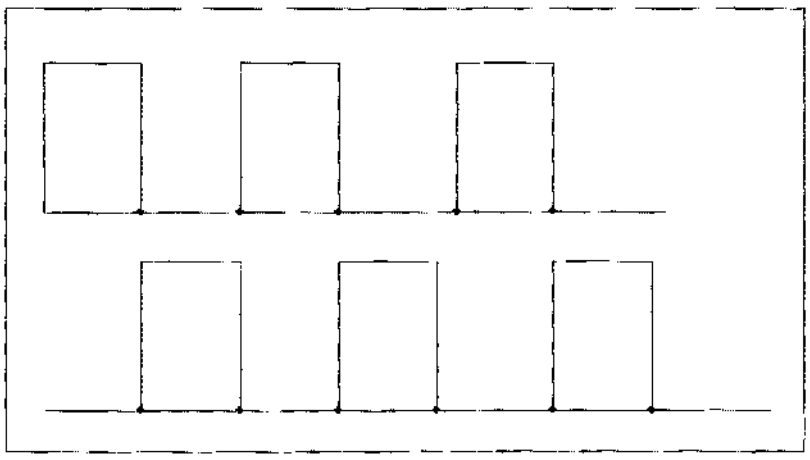


Fig 2.4(a) figure of 50% duty cycle that is harmful for transistor action.

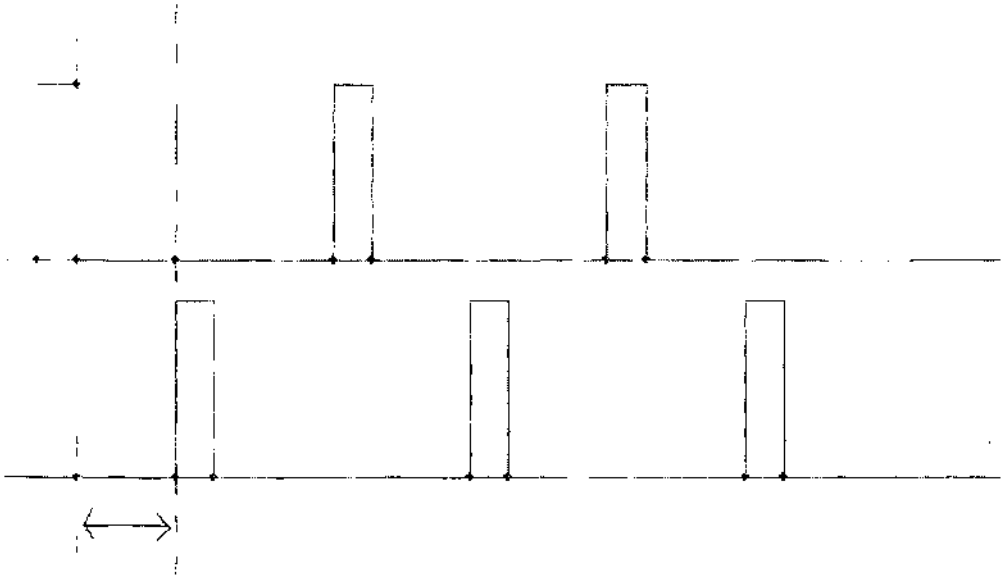


Fig 2.4(b) figure of less than 50% duty cycle that is efficient for transistor action.

The commonly used techniques are [16]:

- Single-pulse-width modulation
- Multiple-pulse-width modulation
- Sinusoidal pulse-width modulation
- Modified sinusoidal pulse-width modulation
- Phase displacement control
- Hysteresis (Bang-bang) pulse-width modulation
- Space Vector pulse-width modulation

The switching functions for the analysis and implementation of the inverter are brought about by a single pulse modulation. The single-pulse-width modulation technique is discussed on the later part [14].

Single pulse width modulation

The gating signals are generated by comparing a rectangular reference signal of amplitude Ar, with a triangular carrier wave of amplitude Ac. The frequency of the carrier wave determines the fundamental frequency of the output voltage. By varying Ar from 0 to Ac, the pulse width 'δ'can be varied from 0 to 180. The ratio of Ar to Ac is the control variable and defined as the modulation index [15].

The modulation index,

$$M = Ar/Ac \quad \ldots\ldots\ldots \text{(vii)}$$

The rms output can be found from

$$Vo = \left[\frac{2}{2\pi} \int_{(\pi-\delta)/2}^{(\pi+\delta)/2} Vs^2 \, d(\omega t) \right]^{1/2}$$

$$= Vs\sqrt{\delta/\pi} \quad \ldots\ldots\ldots \text{(viii)}$$

...er series of the output voltage of Fig: 3.1 may be described as[17],

$$= \sum_{n=1,3,5,....}^{\infty} an \sin(n\,\omega t) + \sum_{n=1,3,5,....}^{\infty} bn \cos(n\,\omega t) \quad \text{volt} \ldots. \text{(ix)}$$

$$= \frac{2}{\pi} \int_0^{\pi} \sin(n\omega t)\ \mathrm{d}(\omega t)$$

$$= \frac{2Vs}{\pi} \int_{(\pi-\delta)/2}^{(\pi+\delta)/2} \sin(n\omega t)\ \mathrm{d}(\omega t) = 4Vs/n\pi \sin(n\delta/2) \ldots\ldots\ldots \text{(x)}$$

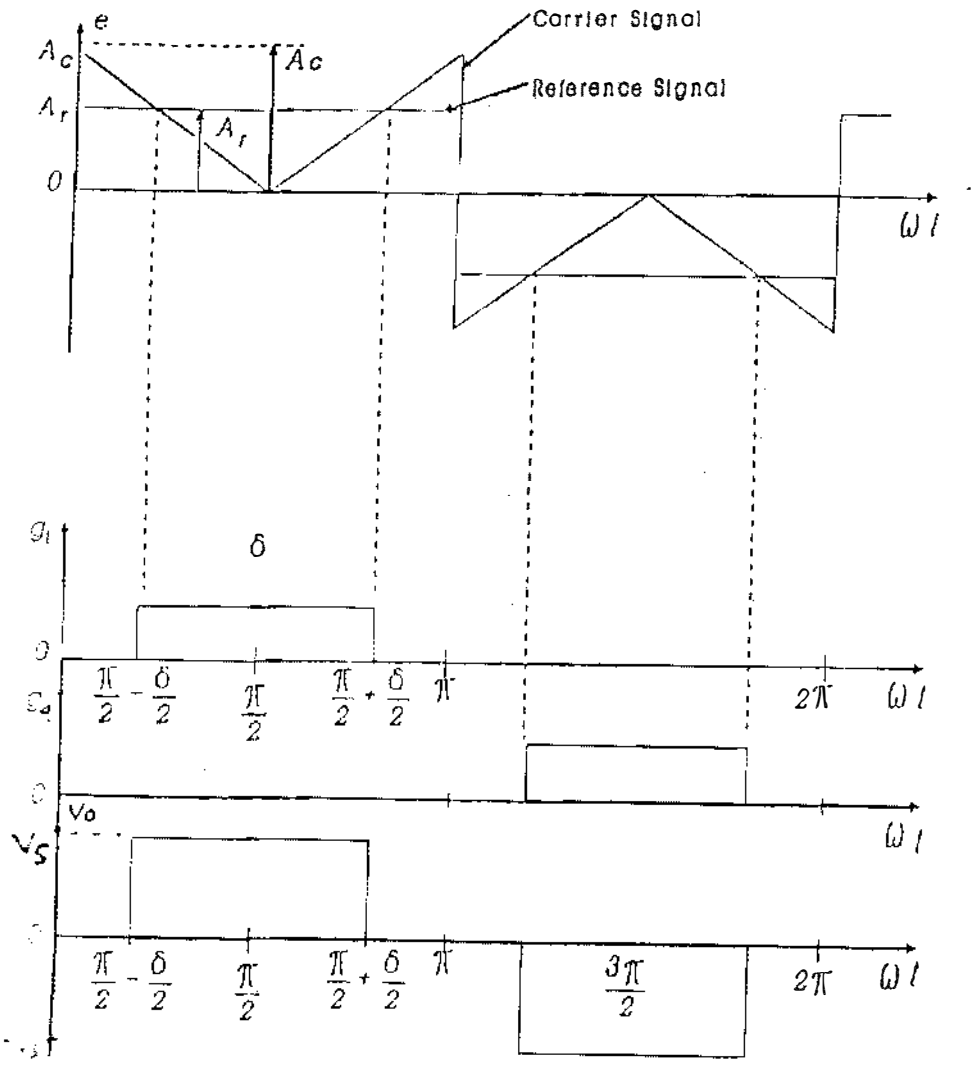


Fig 2.4.1 Single Pulse Width Modulation[19]

$$= 2/\pi \int_0^{\pi} Vs \cos(n\omega t)\ d(\omega t)$$

$$= 2Vs/\pi \int_{(\pi-\delta)/2}^{(\pi+\delta)/2} \cos(n\omega t)\ d(\omega t) = 0 \ldots\ldots\ldots (xi)$$

Thus, Equation 3.1 becomes,

$$V_0(t) = \sum_{n=1,3,5,\ldots}^{\infty} 4Vs/n\pi \sin(n\delta/2) \sin(n\omega t) \text{ volts} \ldots\ldots\ldots (xii)$$

From these curves it may be seen that as 'δ' is decreased, the harmonic content of the output voltage waveform increases until, when the amplitude of the fundamental component has been reduced to 20% of its maximum value, the amplitude of the three harmonics illustrated are very nearly equal to that of the fundamental[17].

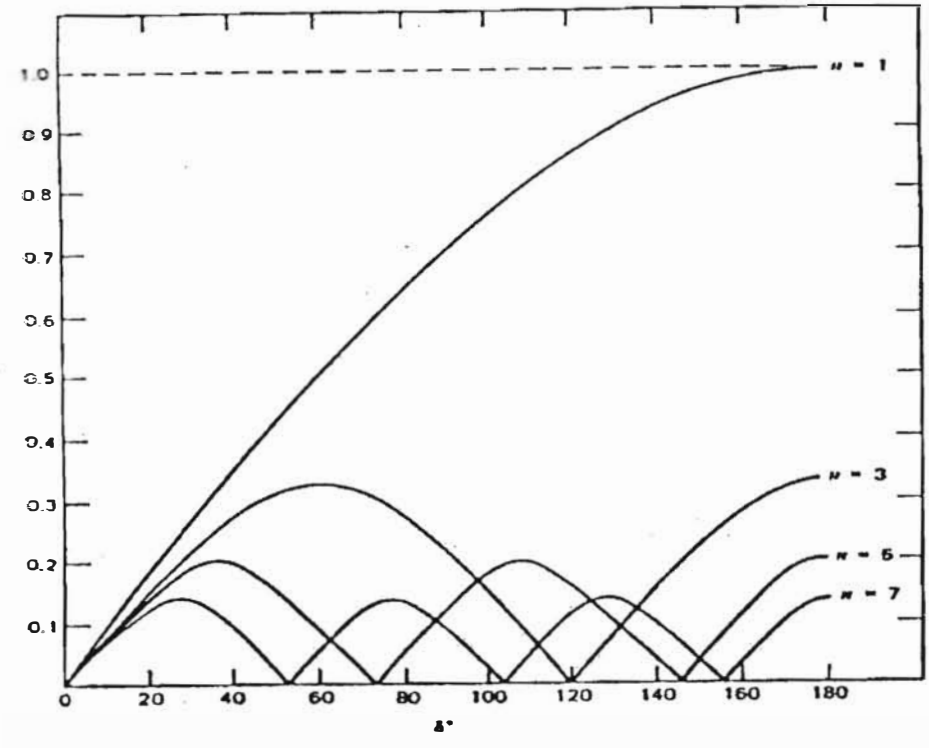


Fig 2.4.2 Harmonic contents of Single Pulse Width Modulation[19]

2.5 Computer Simulations

2.5.1 Introduction

In this section, the proposed method for single phase full bridge inverter has been simulated using the software ORCAD. ORCAD is electronic design automation software. It is usually used to construct electronic schematics and diagrams for simulation purpose. Using this software, the simulation of the whole inverter circuit with load and without load has been carried out so that the values of designed parameter can be obtained for hardware implementation.

2.5.2 Simulated Outputs

For method 1

Schematic diagram of Single phase full bridge inverter with highly inductive load

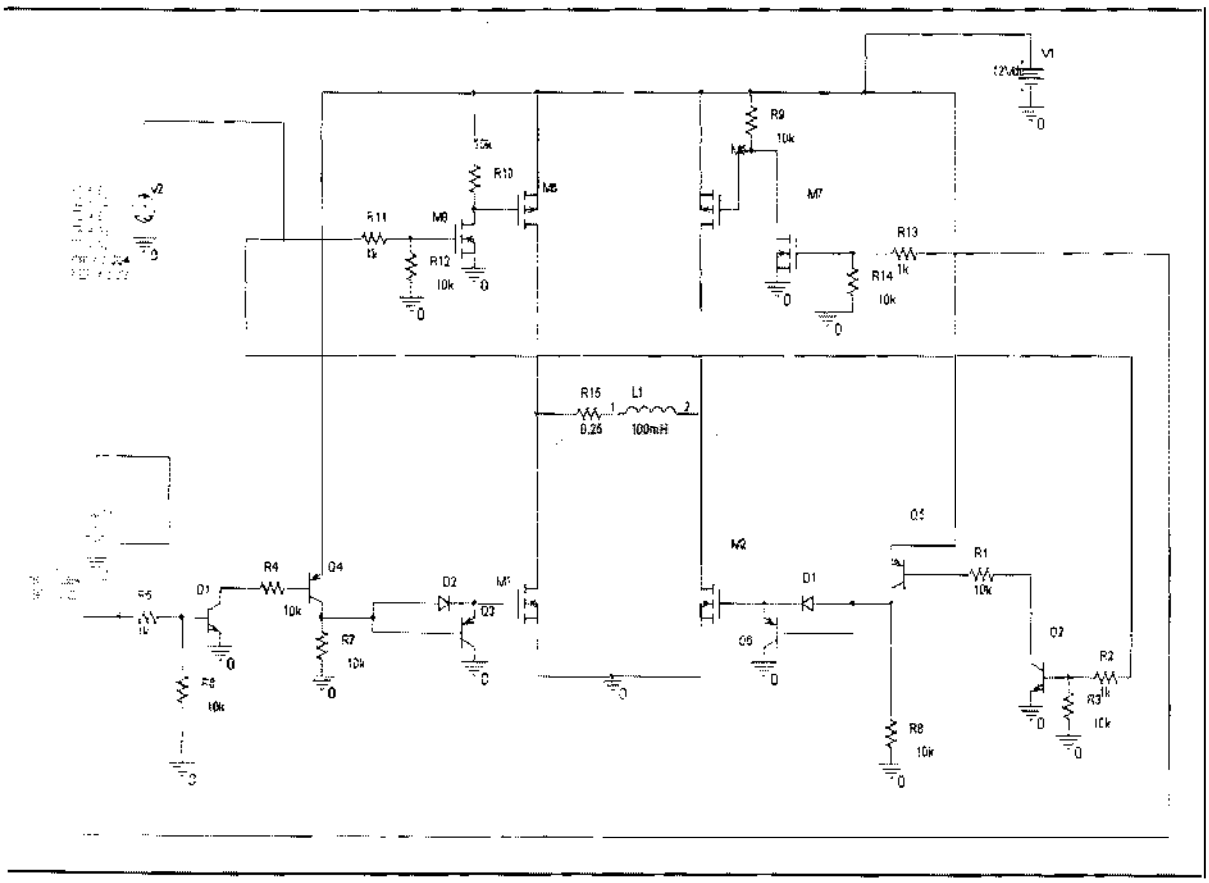


Fig 2.5.2(a)

Output voltage of a single phase full bridge inverter with highly inductive load for 20% duty cycle

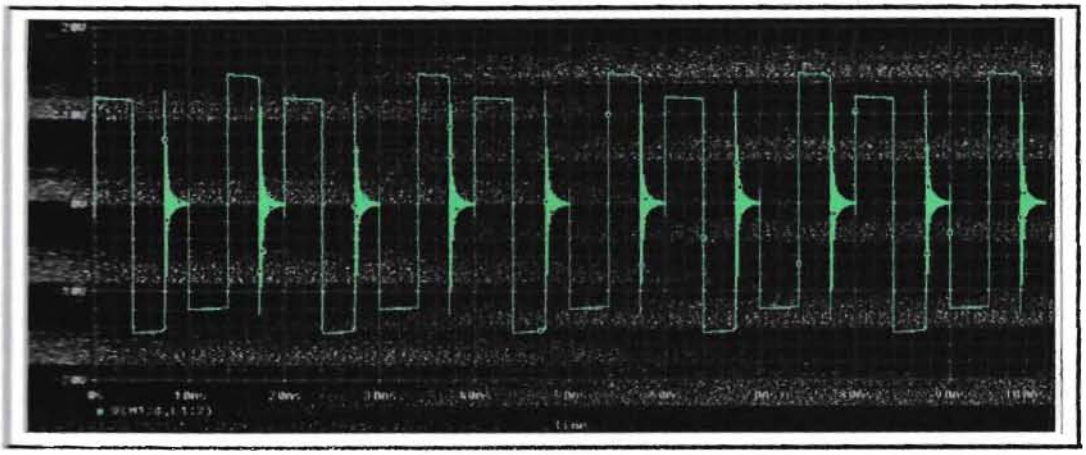


Fig 2.5.2(b)

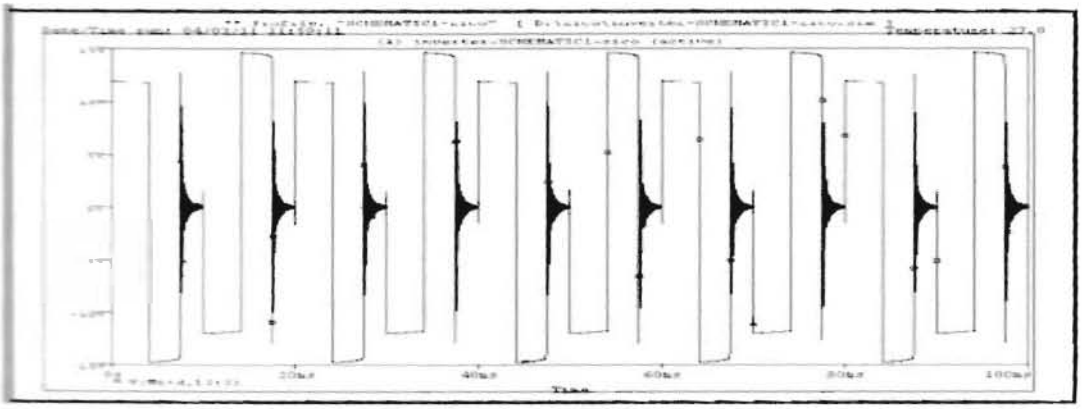


Fig 2.5.2(c)

Harmonic distortion for 20% duty cycle

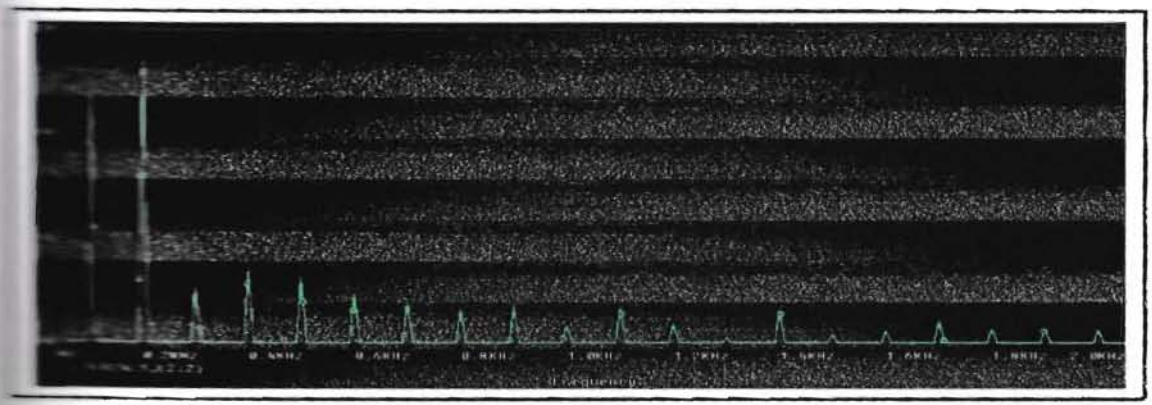


Fig 2.5.2(d)

Output voltage of a single phase full bridge inverter with highly inductive load for 30% duty cycle

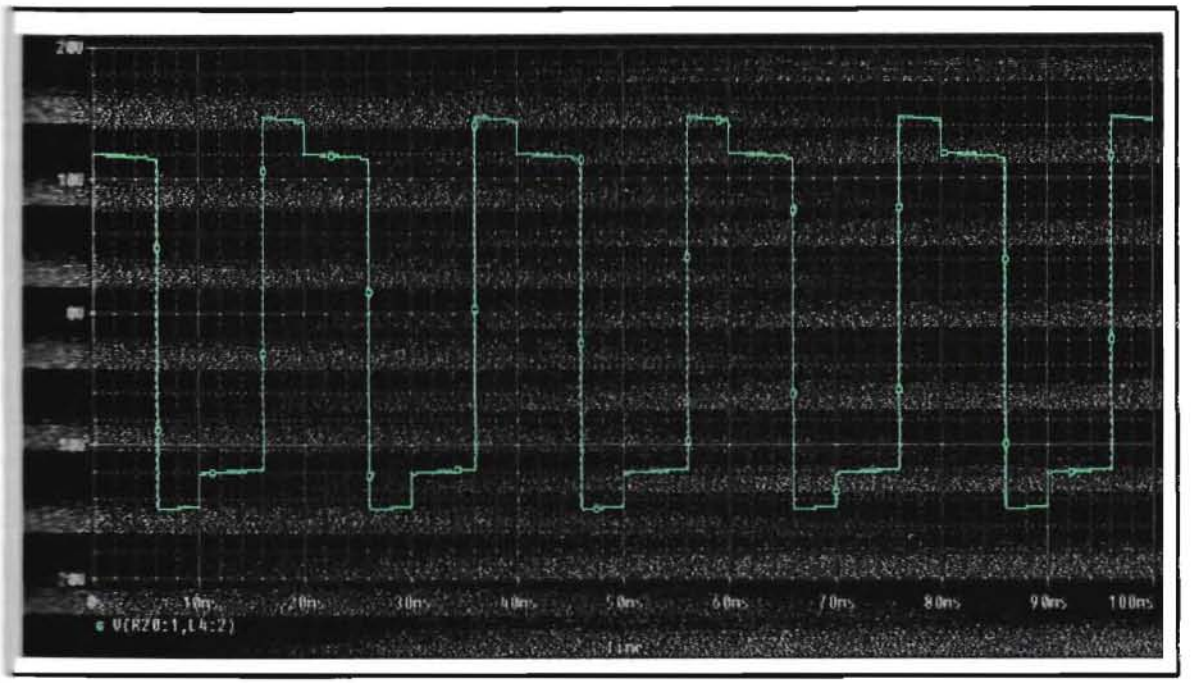


Fig 2.5.2(e)

Harmonic distortion for 30% duty cycle

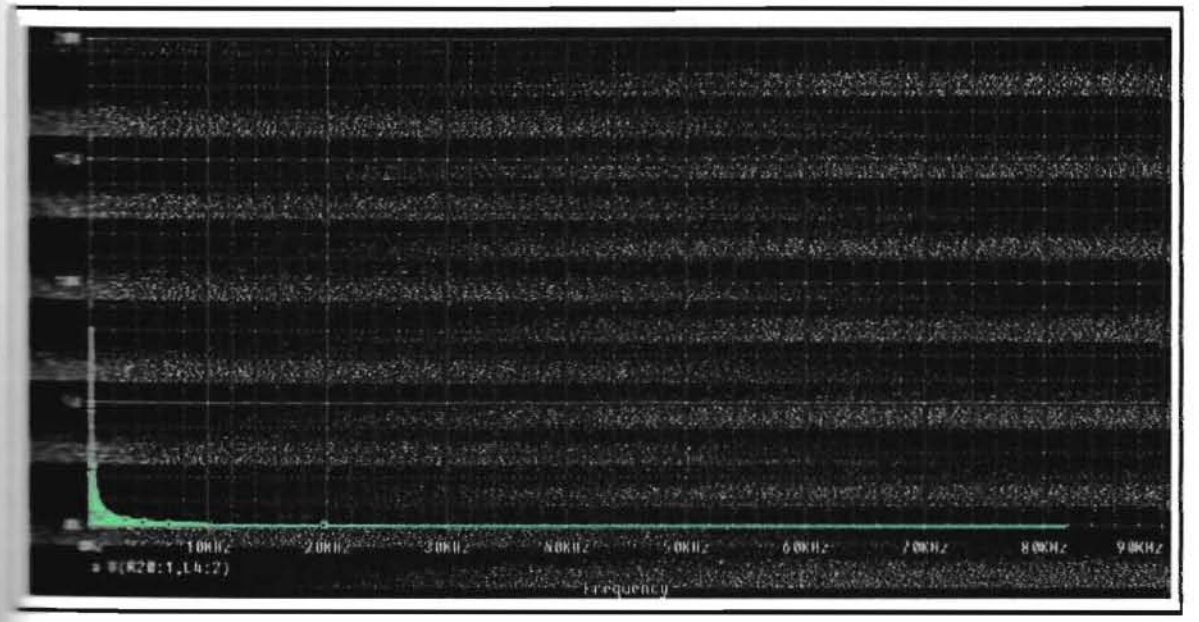


Fig 2.5.2(f)

Output current of a single phase full bridge inverter with highly inductive load

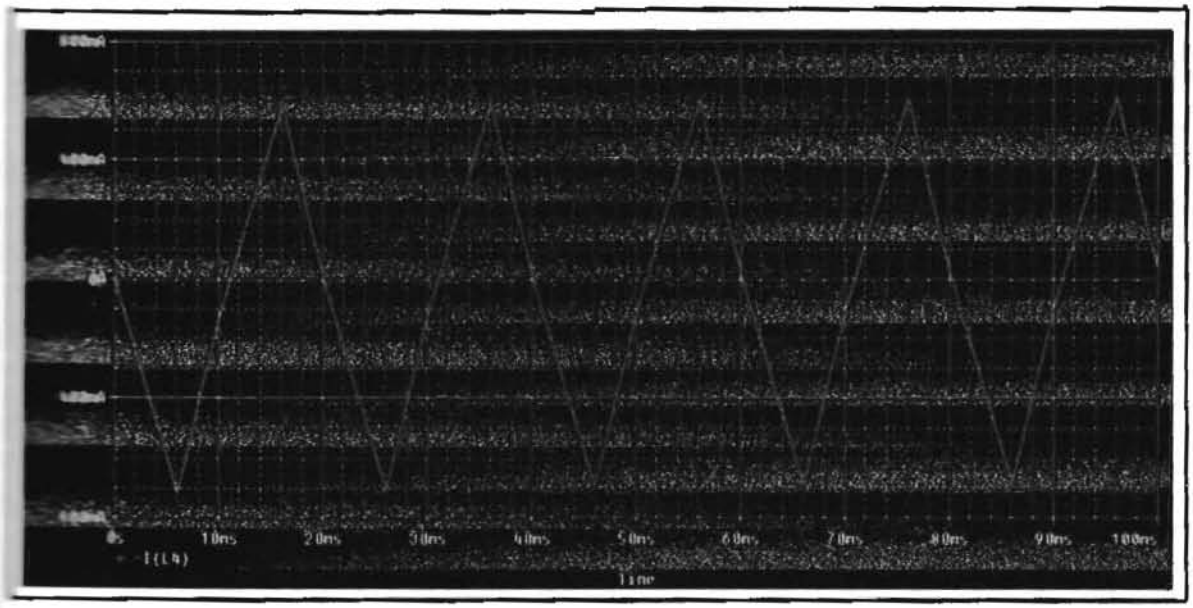


Fig 2.5.2(g)

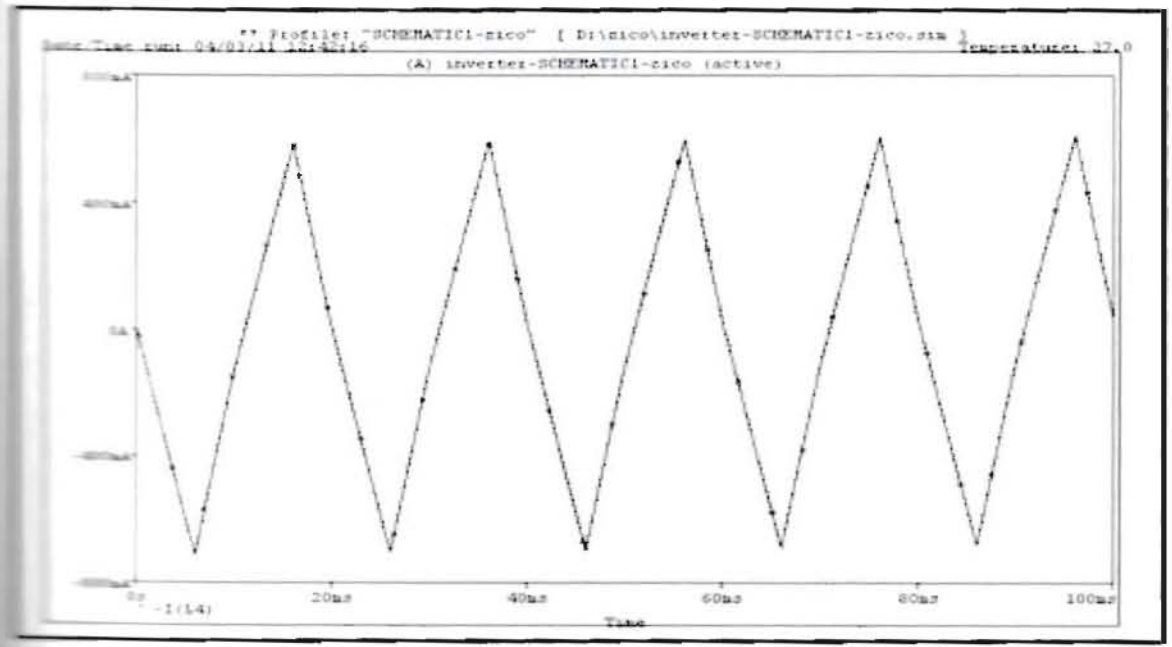


Fig 2.5.2(h)

Schematic diagram of single phase full bridge inverter in no load condition

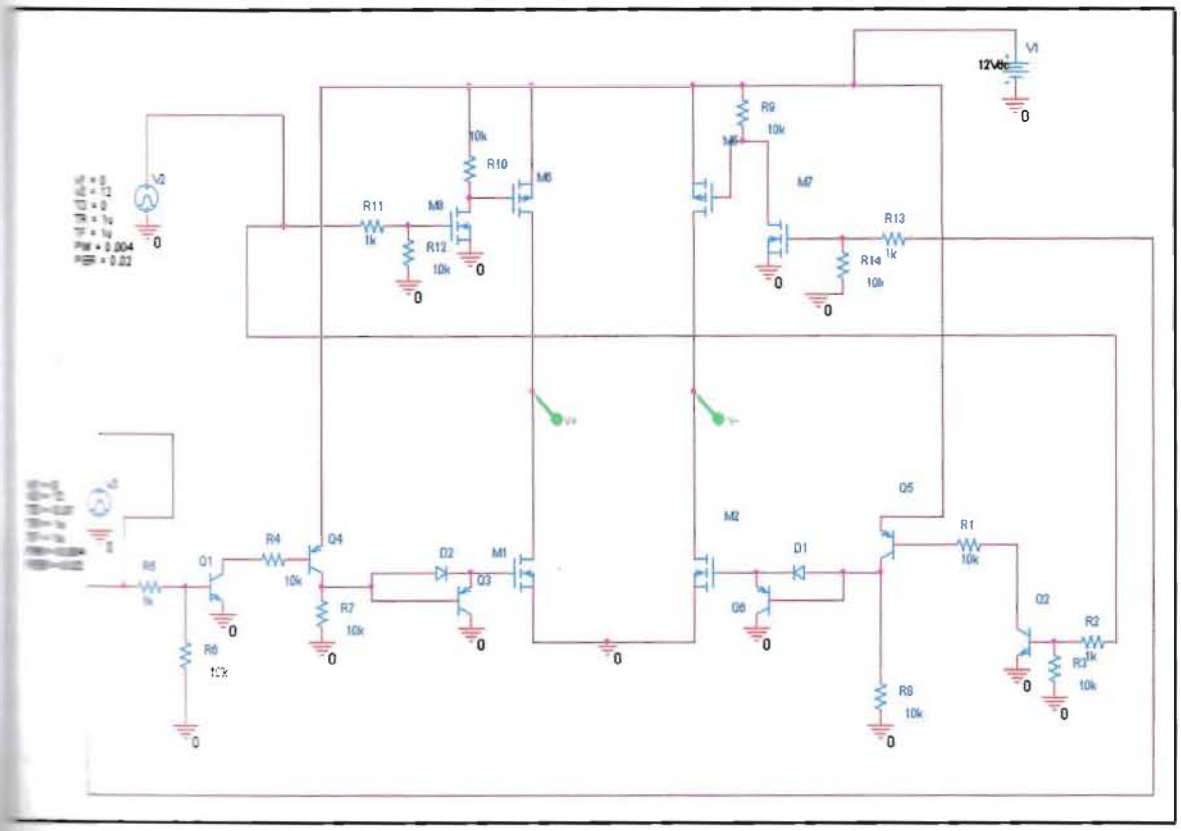


Fig 2.5.2(i)

Output voltage of a single phase full bridge inverter in no load condition

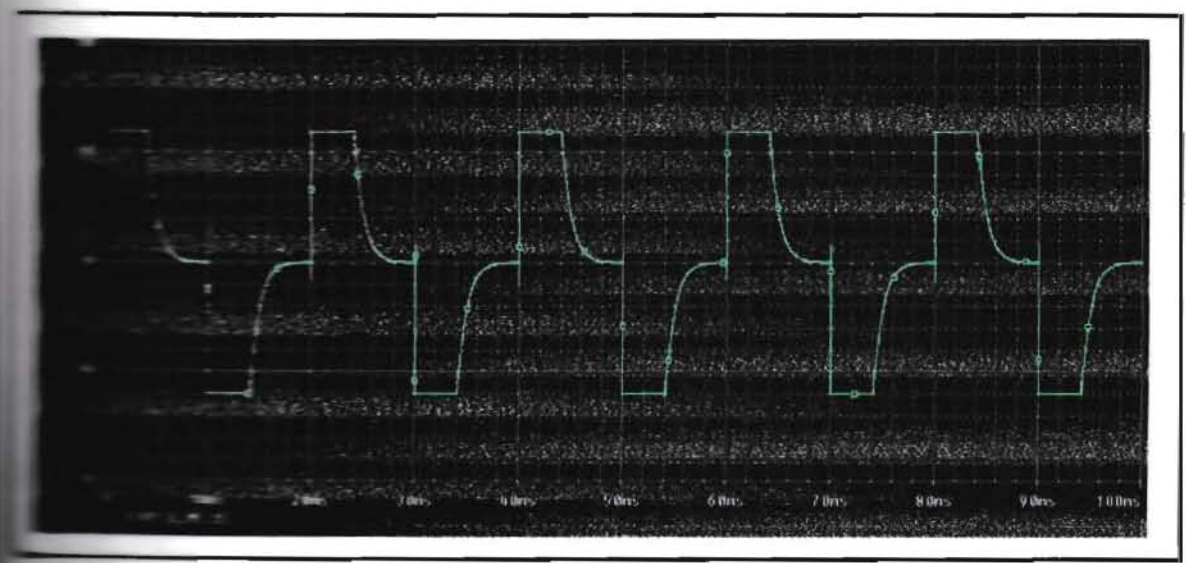


Fig 2.5.2(j)

Schematic diagram of single phase full bridge inverter in no load condition

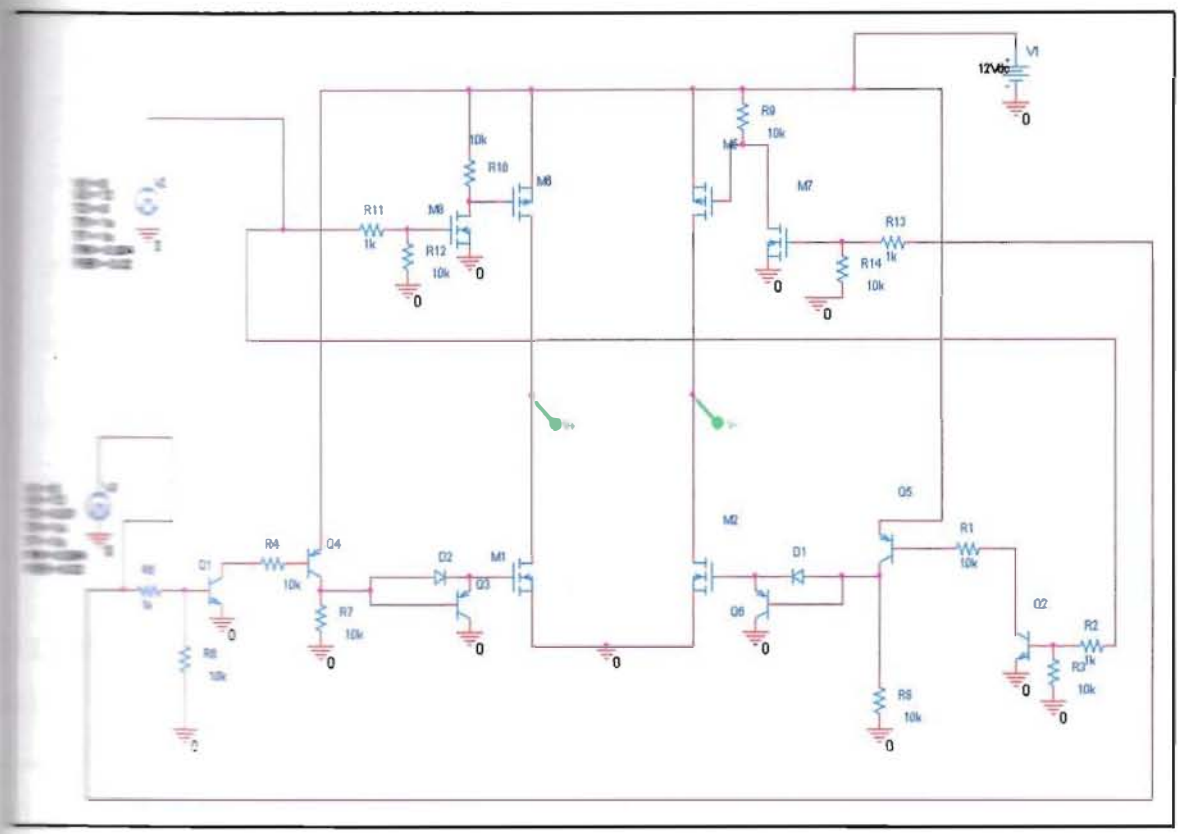


Fig 2.5.2(i)

Output voltage of a single phase full bridge inverter in no load condition

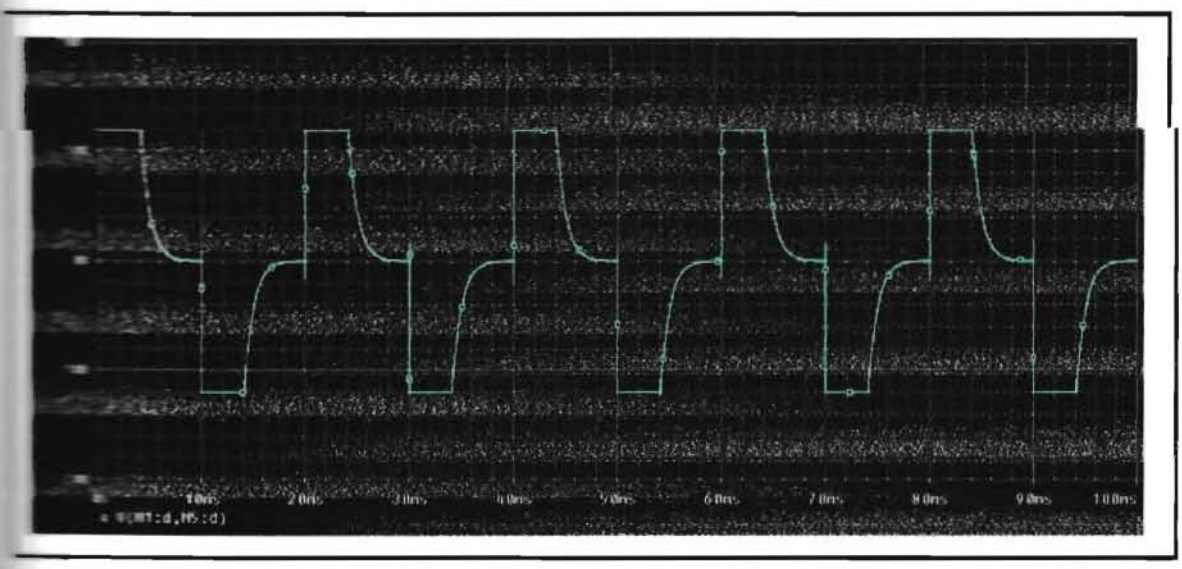


Fig 2.5.2(j)

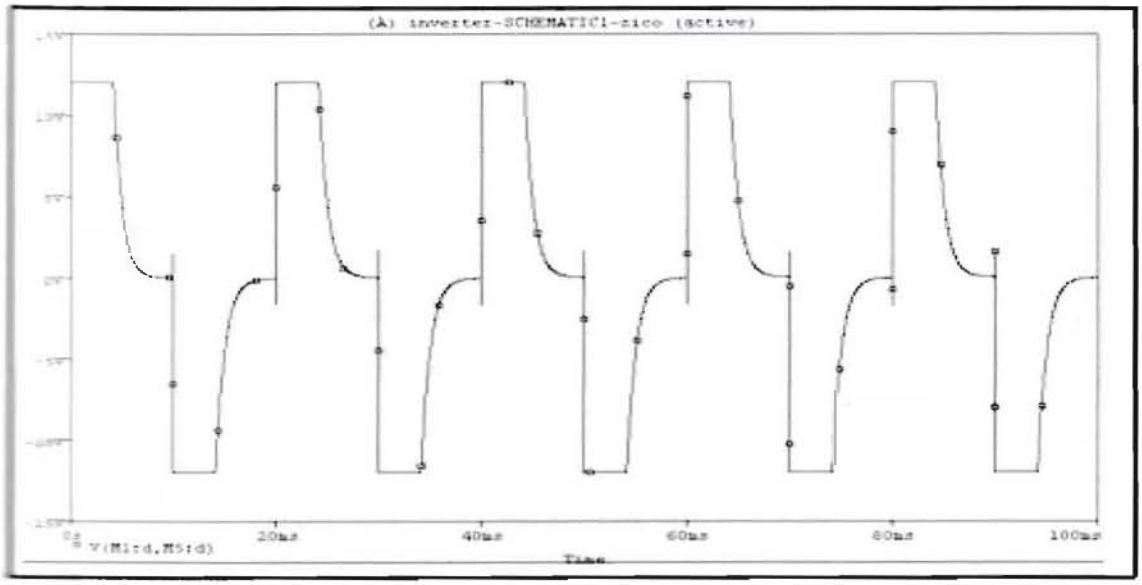


Fig 2.5.2(k)

Schematic diagram of single phase full bridge inverter with transformer and inductive load

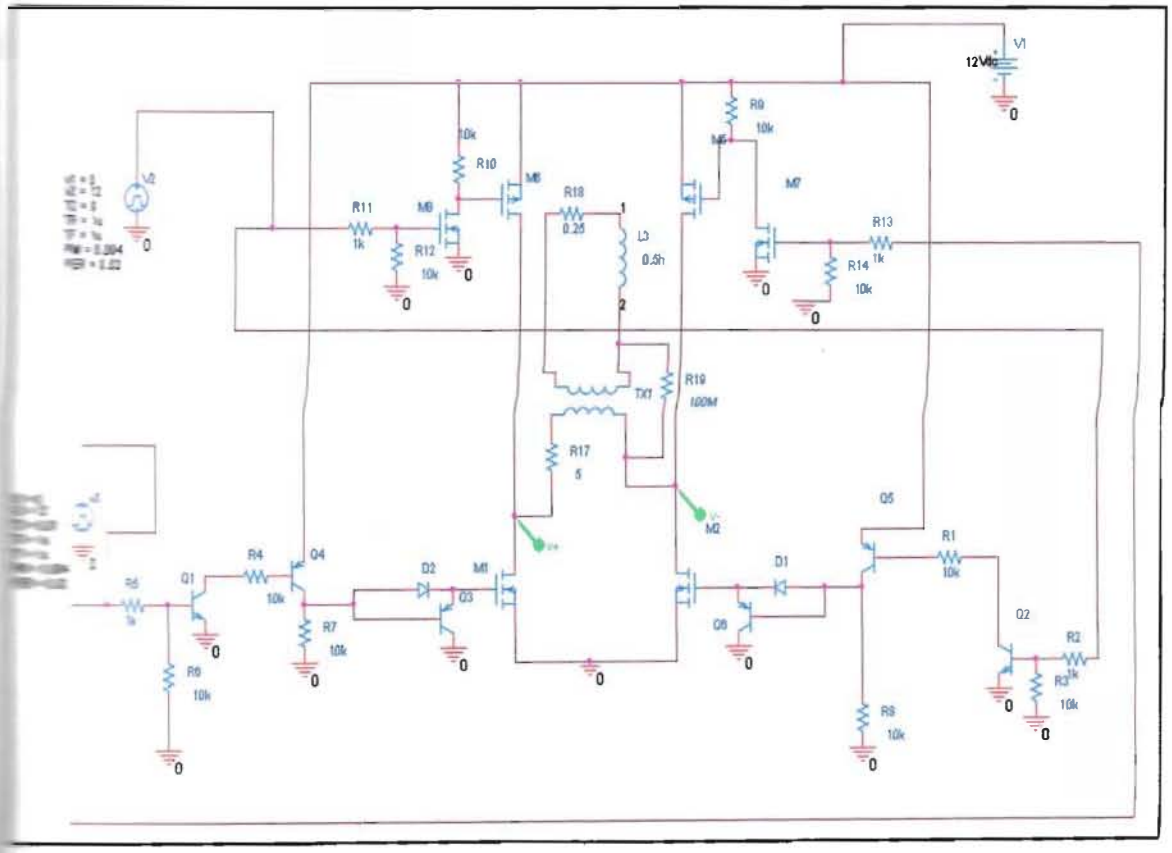


Fig 2.5.2(l)

Primary side output voltage of single phase full bridge inverter with inductive load

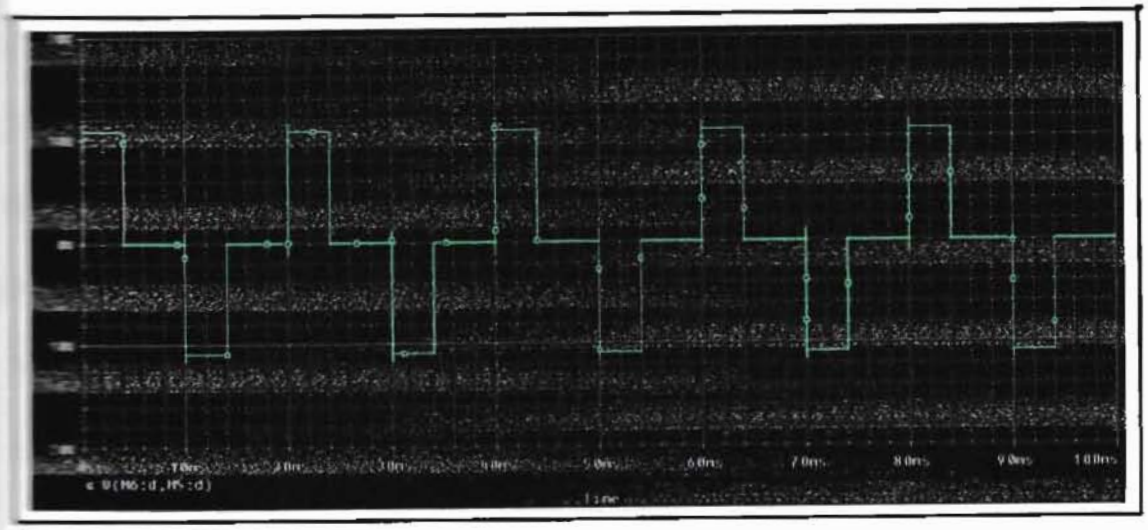


Fig 2.5.2(m)

For method 2

Schematic diagram of single phase full bridge inverter with transformer and inductive load

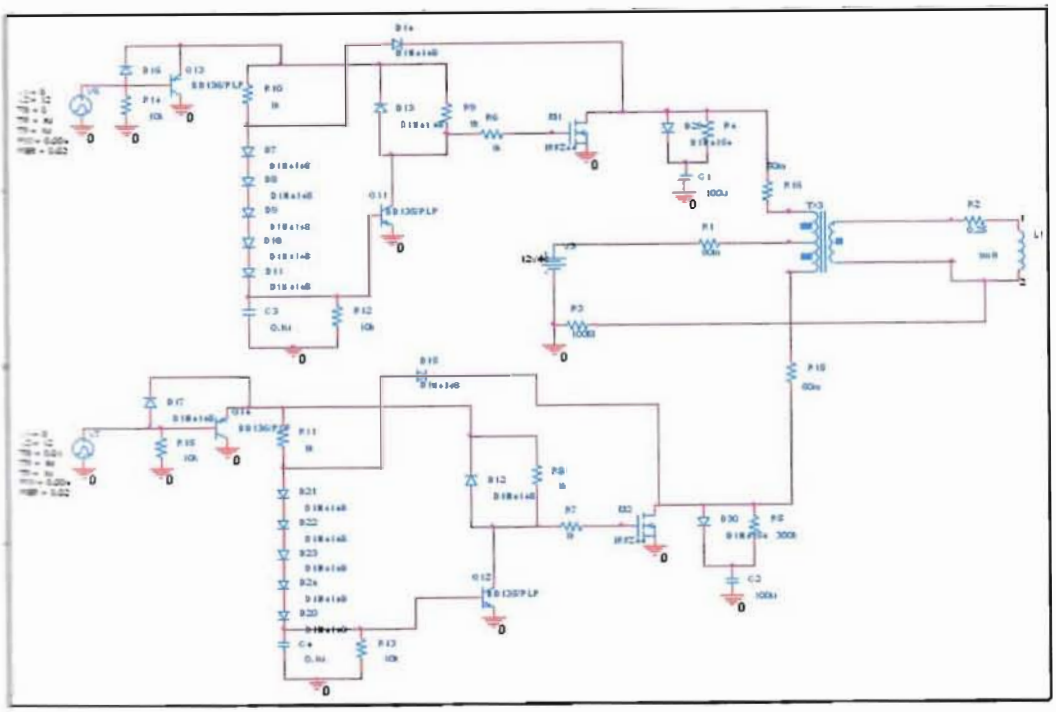


Fig 2.5.2(n)

side output voltage of single phase inverter with inductive load

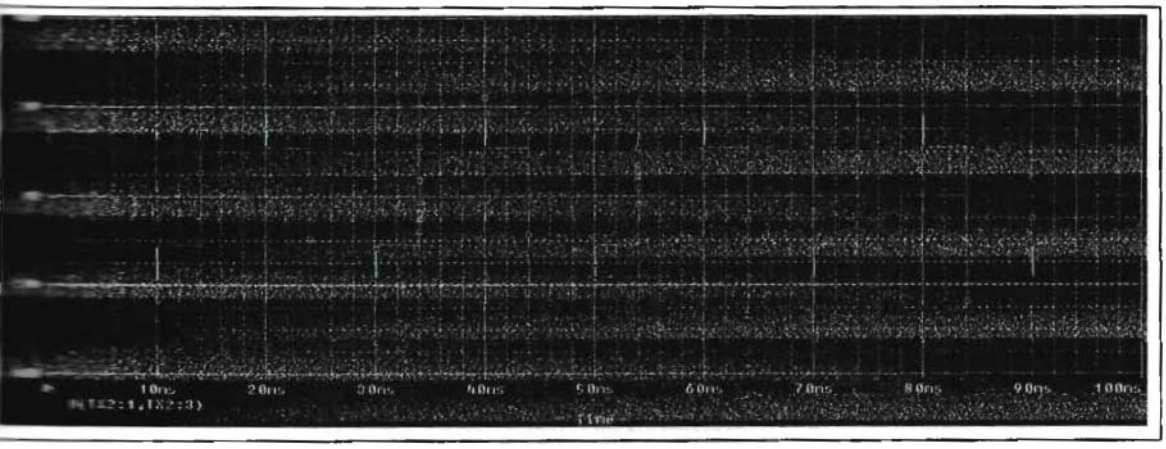


Fig 2.5.2(o)

ic distortion for 20% duty cycle:

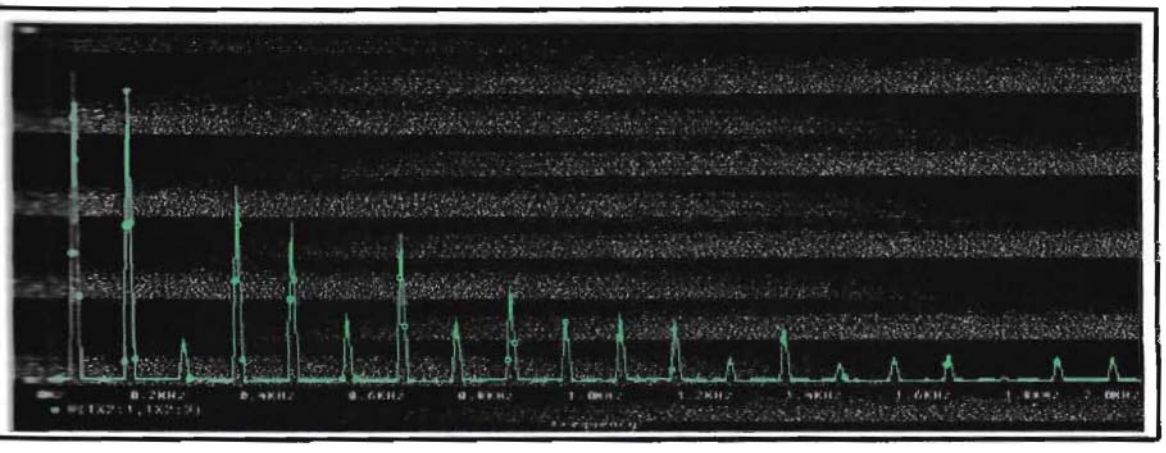


Fig 2.5.2(p)

Summary

principle of operation of a single phase inverter and computer analysis of output voltage input current (with load and without load) for both the two methods is discussed and in this chapter. The output voltage will contain only fundamental frequency if all her harmonics are filtered out.

theoretical analysis is demonstrated by the computer analysis and the computer simulated ults are analogous to the actual input, output waveforms.

CHAPTER 3
DESIGN, CONSTRUCTION AND ANALYSIS

3.1 Introduction

In this chapter, the implementation of the proposed method for single phase full bridge inverter has been discussed. A proper design gives an accurate result. There are many switching devices available to switch on and off in a particular circuit. The important task is to choose suitable devices considering data like power loss, power rating, efficiency etc.

3.2 Functional Description of the Inverter

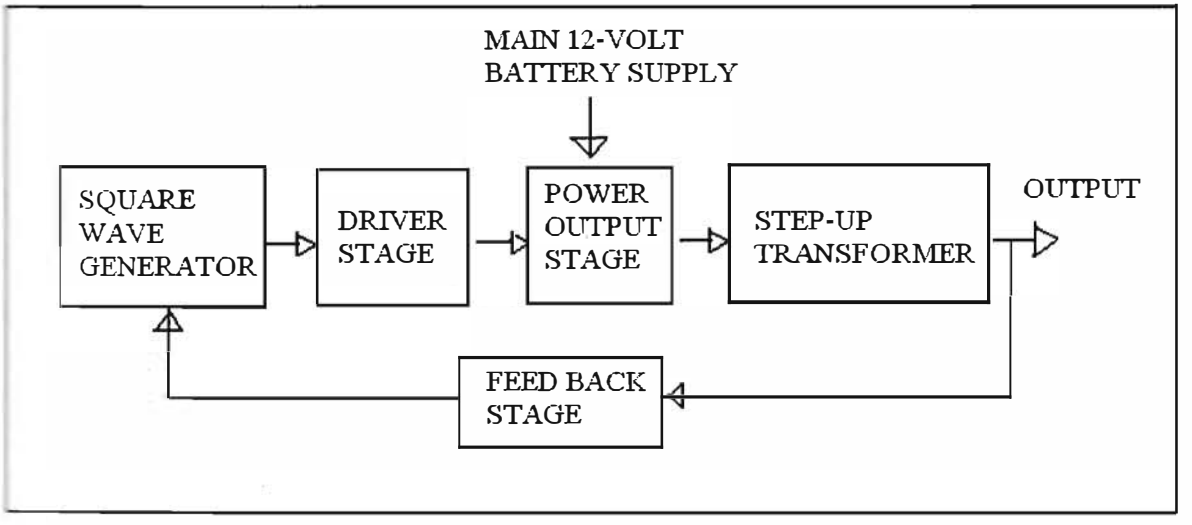


Fig 3.2(a) Block diagram of the inverter

For method 1

The main motive is to supply a 12 volts dc input and obtained a 220 volts Ac output across the load. For that, H-bridge method has been followed. The 12 volts has been supplied from a battery which supplies constant 12 volts dc. At first, 50Hz pulse has been generated using

SG3524 pulse generator .SG3524 is an anti-square wave generator which has two outputs. 180 degree shifted pulse can be obtained from two different outputs. Then, those pulses of amplitude 12 volts were given to the gate of the MOSFETs which were used as switches. Two NMOS and two PMOS have been used for the switching purpose. The PMOS has been used in the high side switching or during positive switching and the NMOS has been used in the low side switching or during negative switching. The MOSFETs here conduct in pairs. As one NMOS and one PMOS conduct as a pairs so we have two pairs here. The gate of each pair has been shorted. Now the generated output pulse from two outputs of the square wave generator has been given to two pairs for conduction. When positive pulse appears at the gate of the MOSFETs, they turn ON and during the appearance of negative pulse they remain OFF. While positive pulse from one output appears to the gate of one pair, they turn ON but at the same time the other pair remains OFF because negative pulse from another output appears at the gate of other pair as anti-square wave has been generated from two outputs. SG3524 has been designed in such a way that it generates the pulses with **dead time** calculation. So, there is no chance for the MOSFETs of same leg turning ON simultaneously.

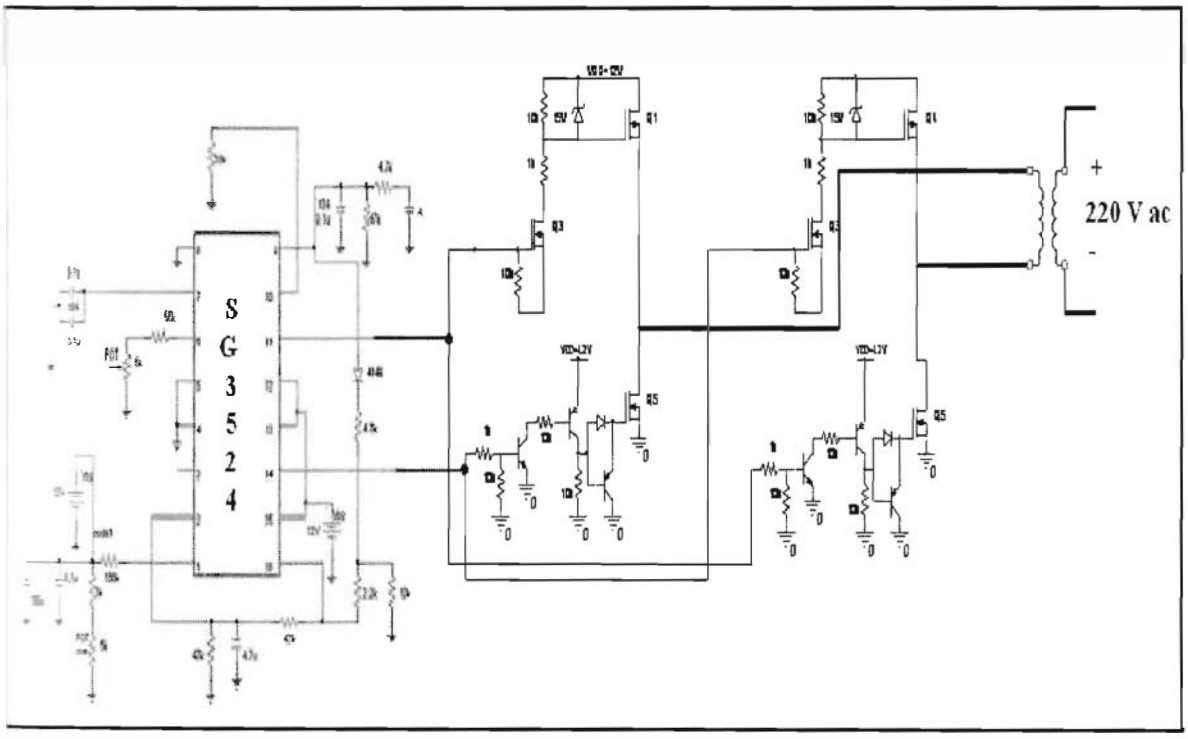


Fig 3.2(b) Schematic diagram of the inverter in method 1

e conduction of the H Bridge MOSFETs produces a 12V ac voltage at the output. The 12V . voltage is fed into a step-up transformer to get a 220V ac voltage at the output of the sformer. A snubber circuit has been used in between the H-bridge and transformer nection. Due to several factors, the ac voltage at the input of the transformer does not in a constant 12V. Due to this variation, the voltage at the output of the transformer es as well. Thus to overcome this voltage variation, a feedback circuit is used from the at to the input of the pulse generator i.e. SG3524.

e feedback is such that an opto-coupler (4N35) is connected from the transformer output to input pin (Vcc) of the pulse generator SG3524. The purpose of the opto-coupler is to te the pulse generator from the 220V high output stage as well as detect any variation in utput.

r method 2

. SG3524 generates a 50Hz pulse which is to be supplied to the MOSFETs. The pulse es out of two output pins of the SG3524, one 180deg shifted from the other.

is method, we have used only two N type MOSFETs for switching at the negative side. positive voltage is directly supplied to the centre pin of the transformer connected at the . While a positive pulse comes to the gate of one MOSFET, a negative pulse arrives at te of the other MOSFET turning it OFF. For this reason, the two MOSFETs cannot be the same time. The circuit diagram is given below,

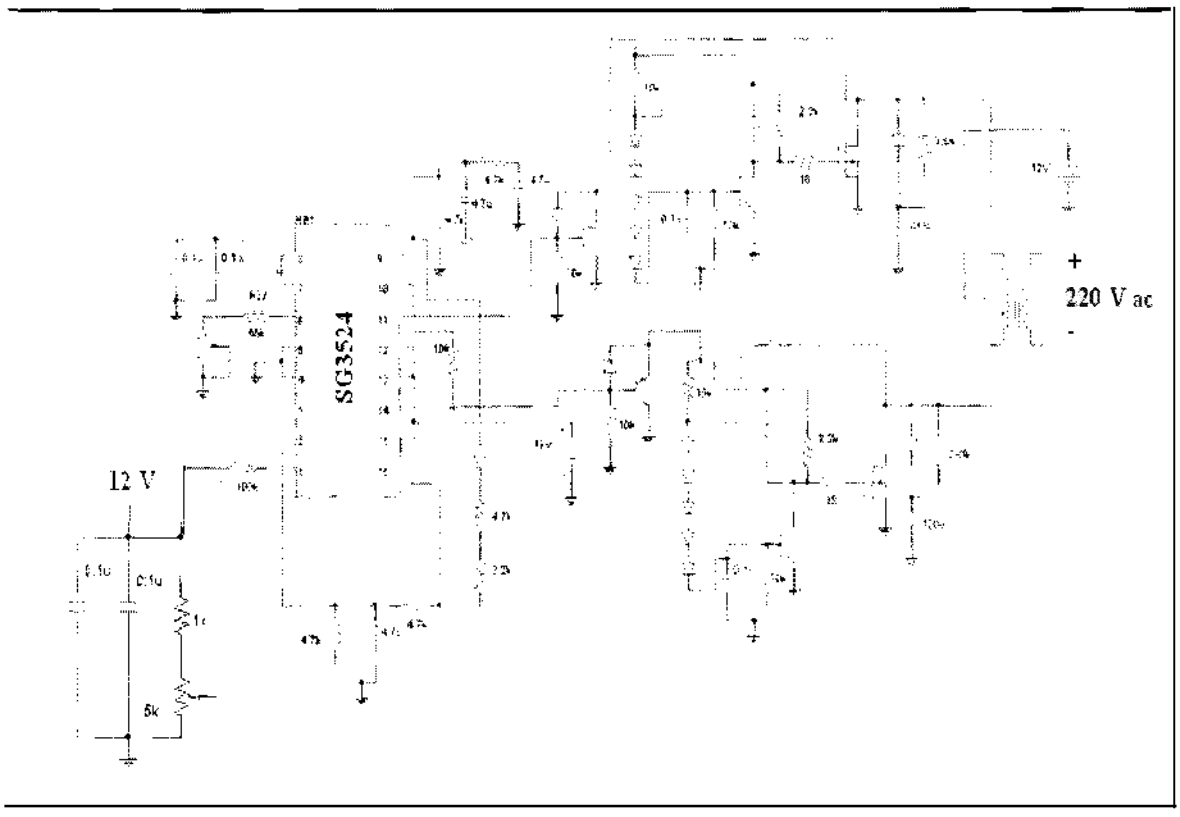


Fig 3.2(c) Schematic diagram of the inverter in method 2

configuration, a MOSFET protection circuit, a Snubber Circuit and a filter circuit is

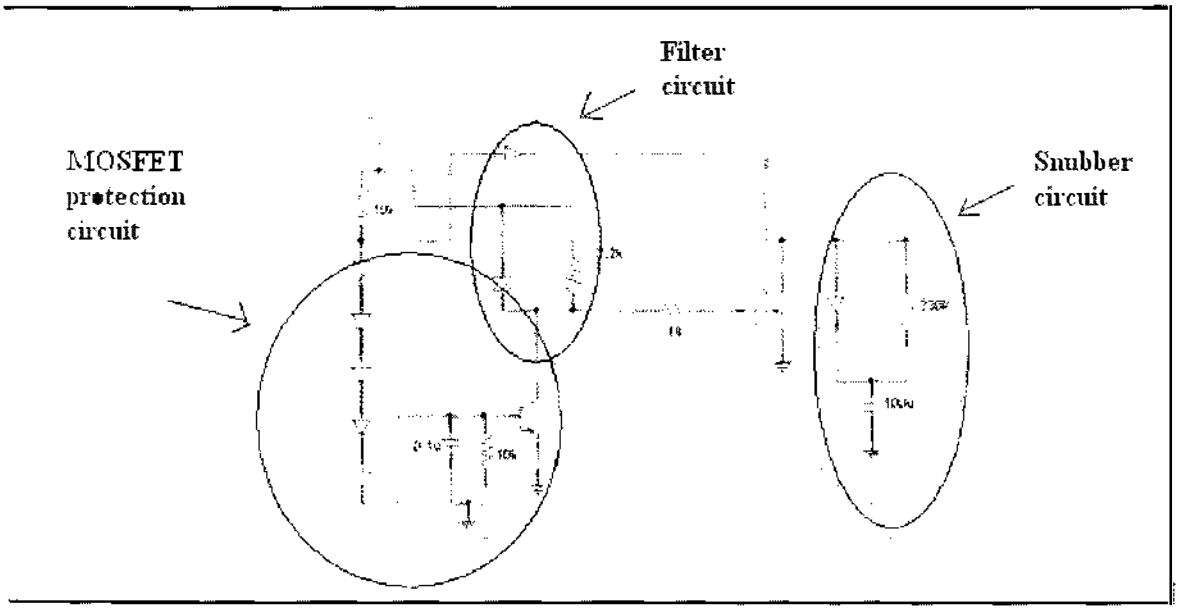


Fig: 3.2(d) Schematic Diagram of MOS Protection, Filter and Snubber circuit

efore the pulse arrives at the MOSFET gate, it passes through a filter circuit where the dth of the arriving pulse is reduced in order momentarily turn the MOSFET ON and OFF ich enables smooth conduction.

hen the MOSFET turns ON, a negative 12 volt appears across one coil of the transformer. a result of the voltage, a back emf is produced at the transformer coil which opposes the rual polarity of the appearing voltage. To minimize the effect of this back emf, the Snubber cuit is used. The Snubber circuit comprises of a diode and a resistor connected in parallel nd a capacitor connected in series with them. It is connected in such a way that when sitive emf is generated the diode is forward biased and the charge goes through it and gets red in the capacitor. When the MOSFET is OFF, the capacitor discharges and neutralizes e back emf.

nother stage is need for this operation, which is MOSFET protection circuit. This circuit is sically used to protect the MOSFET form abnormal voltage. The circuit contains an NPN nsistor; the collector of the transistor is connected to the gate of the MOSFET switch. A apacitor and a resistor are connected in parallel in the base of the transistor. Five diodes are caded and connected in series with the parallel combination of capacitor and resistor. ther diode is connected between the drain of the switch and the edge of the cascaded des. When abnormal voltage appears the diode that connected between drain and cascaded remains forward bias. And let the current flow the cascaded diodes. All the diodes are es that provides 0.6V drop across it, so maximum 3V drop can be occurred here. If the rmal voltage is lower than 3V this series combination will never turns ON, and if it is than 3V all diodes activates and charges the capacitor, which stores this voltage. If the rmal is significant NPN transistor remains ON and by force it OFFs the NMOS switch.

discussion on the designing criteria of power MOSFET is done in a sub-section in this called "power MOSFET choosing". This section highlights how a better power MOSFET can be designed, which does not need any protection circuit during operation.

methods were constructed and after experimentation it was observed that method 1 complexity during high side switching. Besides, in method 2 there was no high side so internal switching loss was comparatively less in method 2 than that of method ethod 2 was a better option in terms of efficiency as well as in terms of complexity. al hardware has been constructed following to method 2 and the design part will be ingly.

3.3 Functional Description of parameters in Internal Blocks

3.3.1 SG3524 Square wave Generator

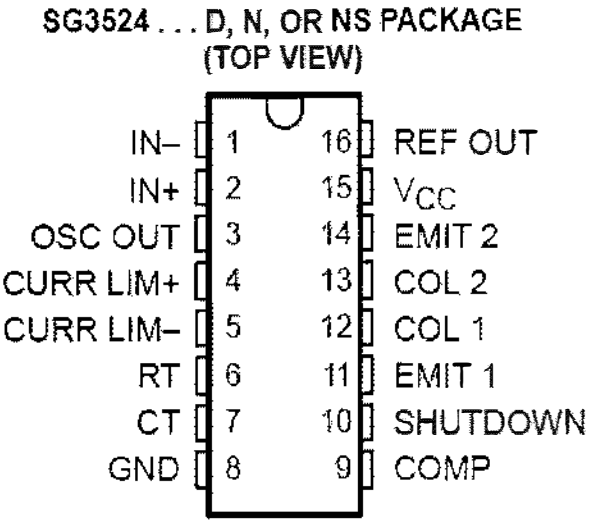


Fig 3.3.1(a) Top view of SG3524

SG3524 incorporate all the functions required in the construction of a regulating power supply, inverter, or switching regulator on a single chip. They also can be used as the control element for high-power-output applications. The SG3524 were designed for switching regulators of polarity, transformer-coupled dc-to-dc converters, transformer less voltage multipliers, and polarity-converter applications employing fixed-frequency, pulse-width modulation (PWM) techniques. The complementary output allows either single-ended or push-pull application. Each device includes an on chip regulator, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted pass transistors, a high-gain comparator, and current-limiting and shutdown circuitry [1].

Functional block Diagram:

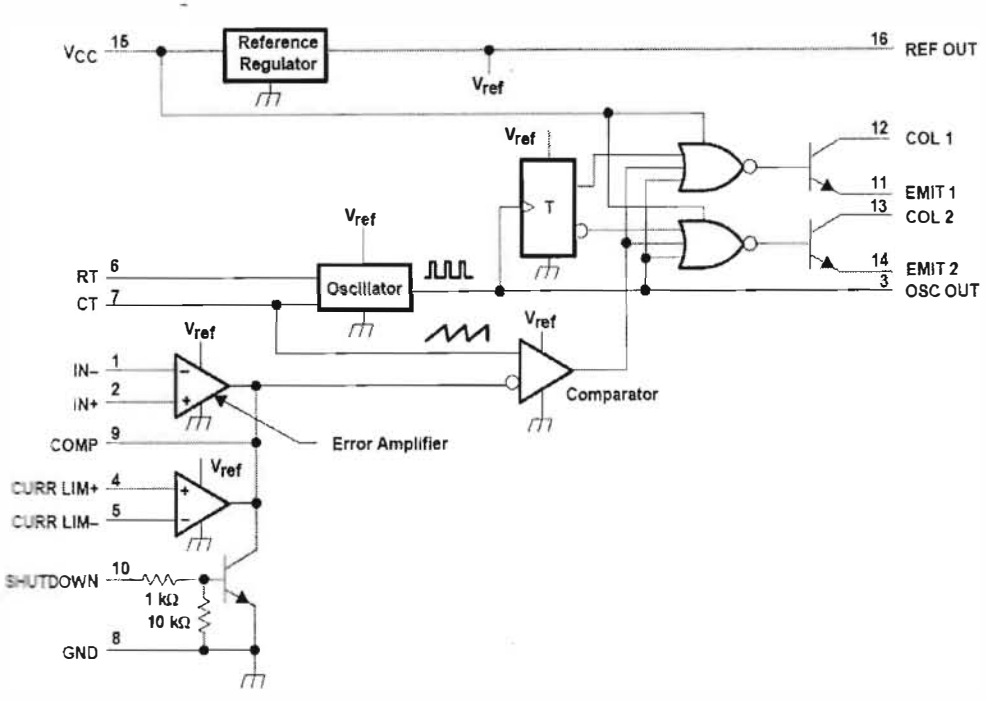


Fig 3.3.1(b) Functional Block Diagram of SG3524

Principle of operation

SG3524 is a 16 pin IC. It has an internal triangular wave generator, which is generated by pin 6 & 7. Pin 6 is basically a timing resistor (RT), which operates on a fixed frequency. Pin 7 is a timing capacitor (CT), RT establishes a constant charging current for CT. This produces a linear ramp at CT, which is fed to the comparator, providing linear control of the output pulse duration (width) by the error amplifier. SG3524 contains a 5V voltage regulator[1]. Pin 15 is Vcc. As Vcc is applied a 5V regulated output appears at pin 16. The internal reference voltage is divided externally by a resistor ladder network to provide a reference within the common-mode range of the error amplifier or an external reference can be used. The output is sensed by a second resistor divider network and the error signal is amplified. SG3524 contains two built-in transistors [2].

Pin 12 and 13 are the collectors of the transistors and pin 11 and 14 are the emitters. The bases of the transistors are internally connected to two 3 input NOR gates. One leg of each of the 3 input NOR gates are connected to the complimentary outputs of a T flip flop. Another

pin of each of the NOR gates are connected to comparator outputs, and another one is connected to an oscillator. Pin 4 and pin 5 are used to limit the current and protect against over load and over current. If no external reference is provided then the amplifier uses an internal reference. If the reference current crosses a particular limit, the SG3524 gets shut down automatically. Pin 10 is the shut down pin which is nothing but a common emitter NPN transistor. If the pin remains high the transistor is ON and shuts down the IC. And if low signal arrives at the pin, the output gets signal [2].

Pin 1 and pin 2 are the inputs of a P controller where pin 1 is a reference input and pin 2 is a feedback input. And the output of the P controller is pin 9.

A signal from CT is compared with the reference voltage to produce a pulse. The signal at the comparator output remains high, until the CT voltage is greater than the reference voltage, otherwise it remains zero.

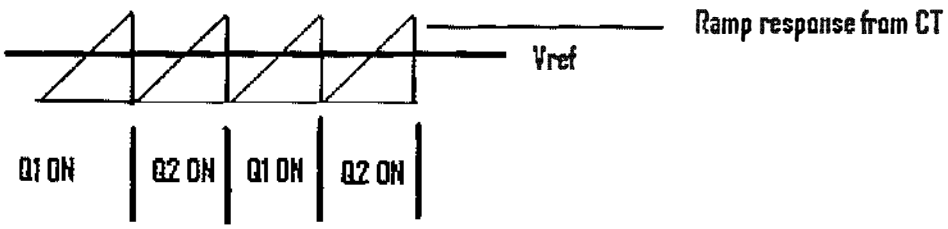


Fig 3.3.1(c) Ramp Response

3524 is designed in such a way that two transistors remain ON in two different periods, which makes an anti phase square output. The transistor gets ON if a high pulse arrives and a square wave at the output is obtained. One advantage of using SG3524 is the duty cycle of the output can be varied.

3.2 Introduction to Power MOSFET

Power MOSFET (metal oxide semiconductor field-effect transistor) is a specific type of MOSFET designed to handle significant power levels[5].

Main advantages are[5]:

i. high commutation speed

ii. good efficiency at low voltages.

iii. easy to drive (as it shares with the IGBT an isolated gate).

The power MOSFET is the most widely used low-voltage (i.e. less than 200 V) switch. It can be found in most power supplies, DC to DC converters, and low voltage motor controllers[5].

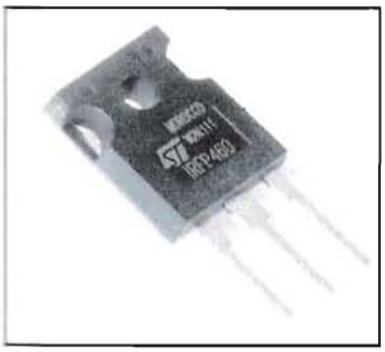


Fig3.3.2(a): Power MOSFET

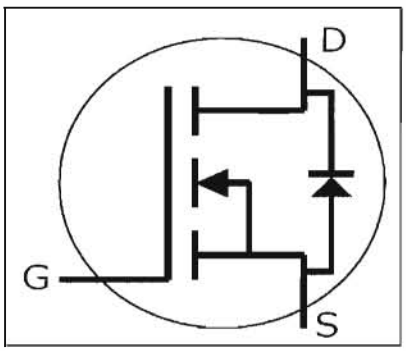


Fig3.3.2(b): Power MOSFET symbol

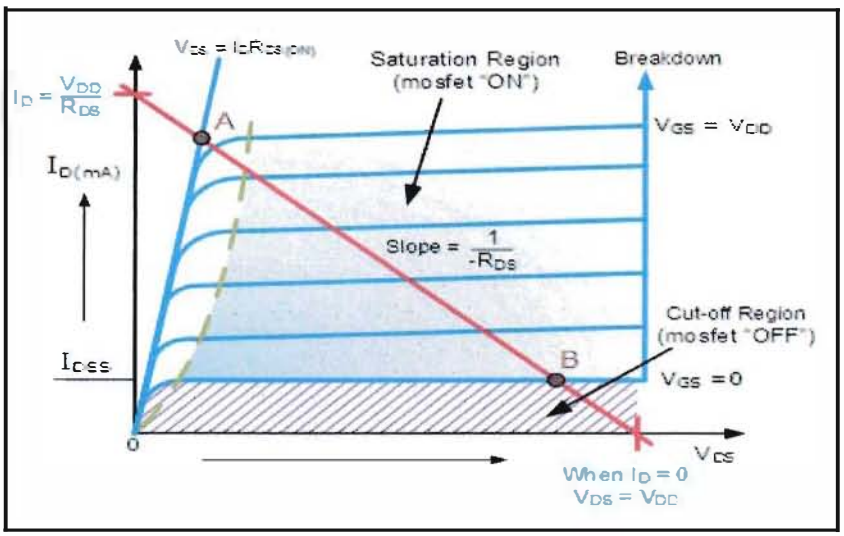


Fig 3.3.2(c): IV characteristics of power MOSFET[6].

Every power devices has two kinds of breakdown states:

i. primary breakdown

ii. secondary breakdown.

i. Primary breakdown usually causes:

1. Over current
2. Over voltage
3. High temperature

or above mentioned problems, power MOSFET is preferable due to its average current ...ing. Power MOSFETs have no reverse bias junction, which means it enables over current ...otection or other way it can be said that it can take momentary or peak current. But ...OSFET is a voltage dependent device so its gate should be sealed [5].

...OSFET does not have the secondary breakdown property because it does not have the ...everse bias junction. As MOSFET has positive temperature coefficient so its temperature is ...portional to the resistivity. As a result it will provide an automatic current spreading. Only ...nction based devices have the secondary breakdown property. As MOSFET is a junction ...e device it can be used in parallel [5].

Power MOSFET choosing

...wer MOSFET is popular for use in switch-mode power supplies, power MOSFETs have ...erating frequencies that are continuously being increased to reduce device size and increase ...wer density [19]. But it results a high di/dt, that make the negative effect stronger from ...rasitic inductance, and causes high-voltage spikes between the power MOSFET drain and ...rce during device turn-off. The spike is even worse during power up because of the empty ...k capacitors and the inductance on the transformer primary side being so low it almost ...als the leakage inductance [19].

...adays robust design of power MOSFETs lets them resist of certain stress levels that ...minate the need for expensive protection circuits, if designers carefully analyze ...formance parameters.

...lanche-mode analysis and junction-temperature estimation are two practical and effective ...ods for choosing the optimal power MOSFET for switching power applications. ...ming to apply these methods will, at the same time, give designers insight into the ...ate balance between cost and reliability [19].

Avalanche-mode analysis

In real applications, overvoltage conditions can be classified into two different groups. One condition is when the power MOSFET's drain-source voltage exceeds the absolute maximum specified, but lower than the device's breakdown voltage. Device then suitability can be determined through junction temperature analysis.

The second condition results when the device breaks down and goes into avalanche mode. During this stage drain-source voltage is clamped to its effective breakdown voltage and the current is commutated through a parasitic anti-parallel diode.

When breakdown occurs, device feasibility in any application is easy to determine using three simple parameters [19]. Those parameters are given as following:

- The peak current through the power MOSFET during avalanche (I_{AS}).
- The junction temperature (T_J) at the start of the unclamped inductive switching (UIS) pulse.
- The time the power MOSFET remains in avalanche (t_{AV}).

Designer can check the UIS capability of the device by plotting I_{AS} and t_{AV} on a graph for a given starting T_J. The plot is given below:

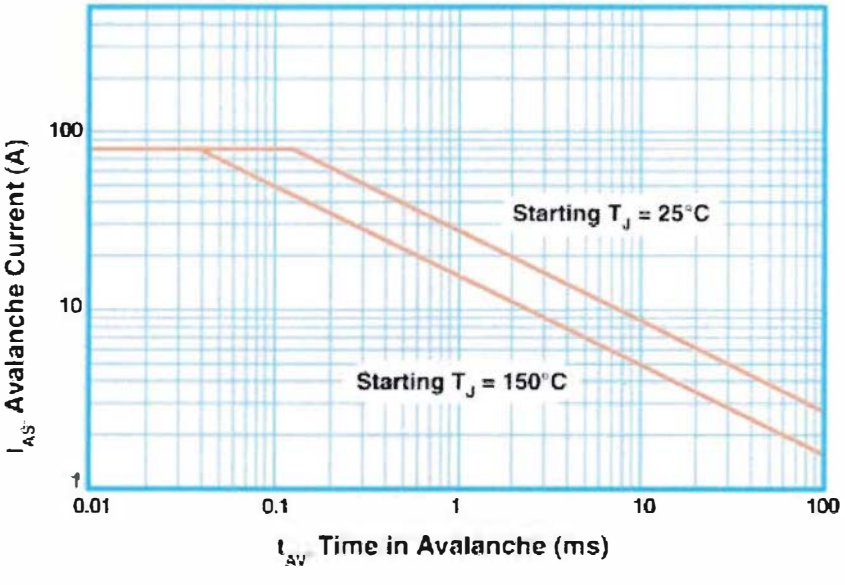


Fig 3.3.2(d) Avalanche mode Curve

g: In a power MOSFET's unclamped-inductive-switching (UIS) safe-operating-area (SOA) graph, the safe operating area is below "Starting T_J = 150°C" line while the area above the Starting T_J = 150°C" line is beyond the devices rating. The area between the two lines requires special considerations [19].

There are three critical areas that known as the UIS safe operating area (SOA) are shown in the above figure:

1 below and to the left of the maximum junction temperature (150°C) line.

2 above and to the right of the 25°C line.

3 between the two lines.

Areas 1 and 2 are easy to determine: either the device is within the UIS SOA rating (1), or beyond the rating (2). When the plot falls into area 3, it is necessary to calculate the junction temperature of the power MOSFET at the start of the UIS pulse to determine applicability.

This graph can also be applied to repetitive pulses through a superposition technique, wherein a UIS pulse is evaluated separately, as if it were a single pulse. Usually, the last pulse in a series of power pulses occurs at the highest junction temperature and, thus, represents the worst stress. If the power MOSFET is within the UIS rating for the last pulse, it is certainly within the UIS ratings for previous pulses which occurred at lower junction temperatures [19].

Estimating T_j

Power MOSFETs breakdowns rarely. If the drain-source voltage exceeds the absolute maximum rating it occurs. The drain-source breakdown voltage (BV_{DSS}) of a power MOSFET has a positive temperature co-efficient, so as temperature rises, a higher voltage is required to cause breakdown [19].

According to the Fairchild data FQA11N90C 900-V MOSFET (MOSFET package) has a temperature coefficient of 1.02 V/°C, so at 120°C its BV_{DSS} reaches about 990 V. In many cases, the ambient temperature during MOSFET operation is over 25°C and the power loss

causes the junction temperature of the power MOSFET to rise above the ambient temperature.

In a real breakdown condition, the drain current reaches a much higher level and the breakdown voltage is even higher than the above value. For practical purposes, breakdown voltage in real applications is calculated at 1.3 times the rated low-current breakdown voltage [19].

Even though the abnormal voltage spike did not cause a device breakdown, the junction temperature of the power MOSFET should be kept below the specified maximum junction temperature to ensure reliability. The steady state junction temperature can be expressed as:

$$T_j = P_D R_{\theta JC} + T_C$$

Where T_J is the junction temperature, T_C the case temperature, P_D the power dissipated in the junction, and $R_{\theta JC}$ the steady-state thermal resistance between the junction and case of the MOSFET.

In our proposed methods, the power MOSFETs that have been used are:

1. IRF Z44 N Channel MOSFET
2. IRF 9520 P Channel MOSFET

3.3.2.1 IRF Z44 N Channel MOSFET

IRF Z44 is an advanced power MOSFET. It can handle current up to 50A and drain to source voltage up to 60V. IRFZ44 have the following features:

- Avalanched rugged technology.
- Rugged gate oxide technology.
- Low input capacitance
- Improved gate charge.
- Extended safe operating area.
- High operating temperature.
- Low leakage current: 10uA (MAX) at V_{DS} = 60V.

- Lower channel on resistance $R_{DS(ON)} = 0.020\Omega$.

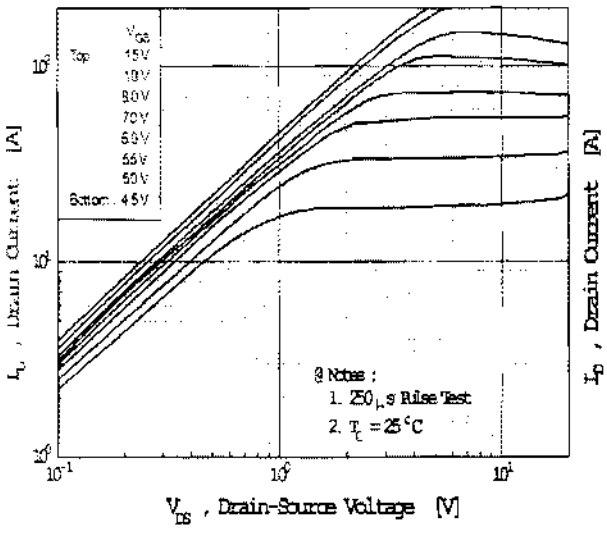


Fig 3.3.2.1(a): IV characteristics

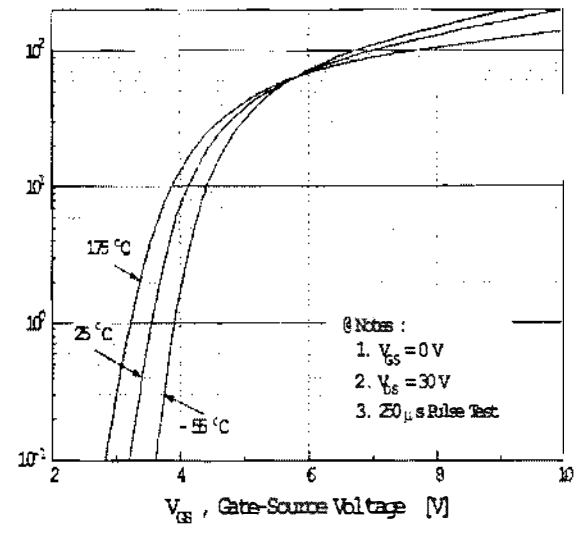


Fig 3.3.2.1(b): Transfer characteristics

3.3.2.2 IRF9520 P channel MOSFET

IRF9520 P channel MOSFET is an advanced power MOSFET. It is designed for high power bipolar switching transistors which require high speed and low gate drive power. It can handle current up to 6A and drain to source voltage up to 100V. It requires a minimum channel on resistance of 0.6Ω[4].

IRF9520 has the following features:

- Designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation.
- Single Pulse Avalanche Energy Rated.
- Nanosecond Switching Speeds.
- SOA is Power Dissipation Limited.
- Linear Transfer Characteristics.
- High Input Impedance.

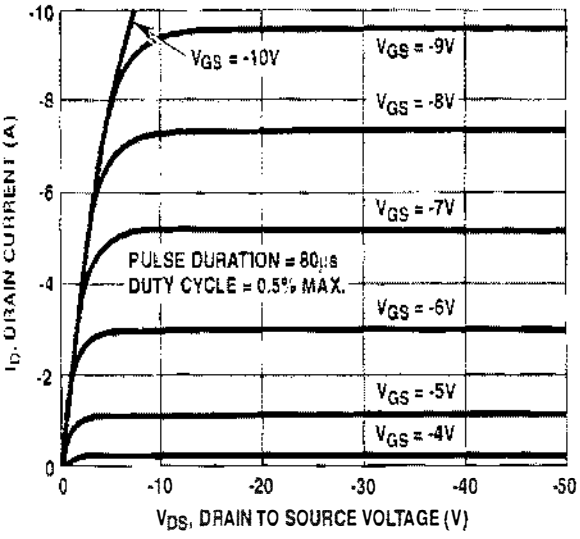


Fig 3.3.2.2(a): IV characteristics[3]

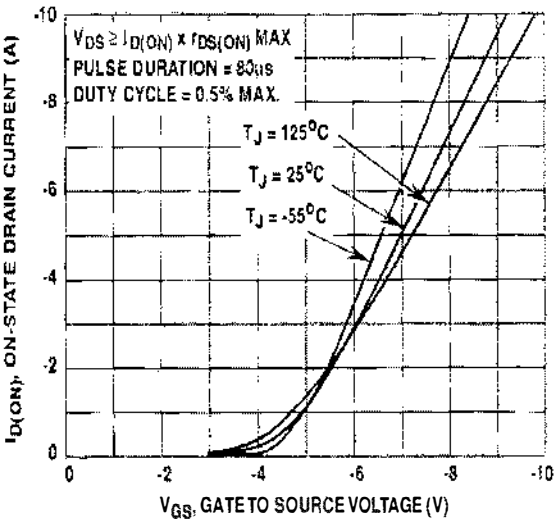


Fig 3.3.2.2(b): Transfer characteristics[4]

3.3.3 Driver circuit

s the MOSFETs that have been used for switching are power MOSFETs, the driver circuits ve been chosen in such a way that they can drive those power MOSFETs with ease.

Power-MOSFET gate driver

er-MOSFET gate driver is a power amplifier that produces a high current gate drive for a er MOSFET from a low power input of a controller IC. It is required when a PWM roller cannot provide the output current required driving the gate capacitance a power SFET. Gate drivers may be implemented as dedicated ICs, discrete transistors, or sformers. Partitioning the gate-drive function off the PWM controller allows the roller to run cooler and be more stable. It is done by eliminating the high peak currents eat dissipation needed to drive a power MOSFET at very high frequencies [8].

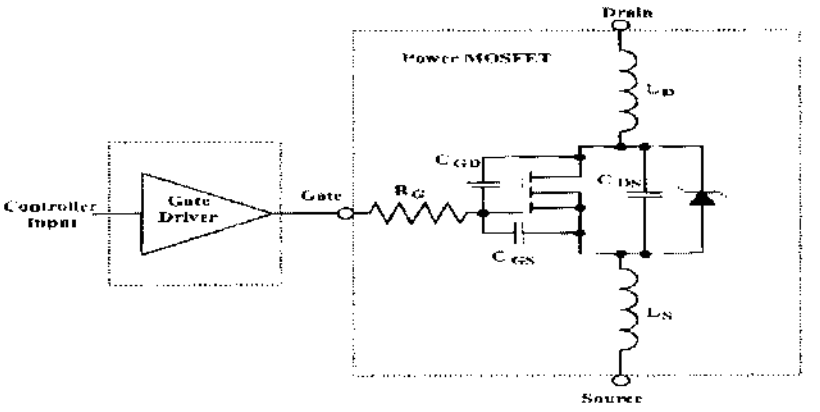


Fig: 3.3.3(a) Power MOSFET gate driver

Fig 3.3.2.8: Equivalent circuit showing components that have greatest effect on switching.

A simplified model including the parasitic components that influence high-speed switching, gate-to-source capacitance (CGS), the gate-to-drain capacitance (CGD), and drain-to-source capacitance (CDS) is shown in the figure above. Values of the source inductance (LS) and drain inductance (LD) depend on the MOSFET's package. The other parasitic component is RG, the resistance associated with the gate signal distribution within the MOSFET that affects switching times [9].

An important attribute for the gate driver is its ability to provide sufficient drive current to quickly pass through the Miller Plateau Region of the power-MOSFET's switching transition. Miller Plateau Region: In the gate charge characteristics curve a flat horizontal portion is observed which the so called Miller Plateau Region). When the device switches, the gate voltage is actually clamped to the plateau voltage and stays there until sufficient charge has been added or removed for the device to switch. It is useful in estimating the driving requirements, because it tells that the voltage of the plateau and the required charge to switch the device. Thus the actual gate drive resistor can be calculated, for a given switching time [ ].

This region occurs when the transistor is being driven on or off, and the voltage across its gate-to-drain parasitic capacitor (CGD) is being charged or discharged by the gate driver.

Figure 2 plots total gate charge as a function of the gate-drive voltage of a power MOSFET.

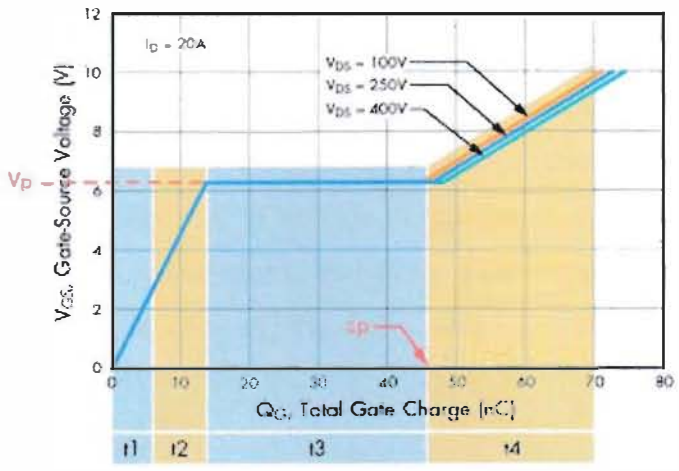


Fig 3.3.3(b) Gate Charge vs Vgs of a Power MOSFET[10]

Driver circuit is also required because the Power MOSFET switches in their non conducting condition are subject to a spurious turn-on if the drain source voltage changes abruptly. These voltage variations usually occur in a very noisy environment. These spurious transitions are subject to both external circuit conditions and to parasitic elements of the MOSFET power switch itself. While an unwanted transition of the MOSFET from on-state to off-state may be damaging to the performance of the overall power system, a spurious transition from off-state to on-state is frequently very severely damaging to the MOSFET power switch itself and in certain instances may cause its immediate destruction[7].

3.3.4 Optocoupler (4N35)

Optocoupler is basically an electronics device that isolates a particular side of the circuit from high or rapidly changing voltage side. Electronic equipment and signal and power transmission lines can be subjected to voltage surges induced by lightning, electrostatic discharge, radio frequency transmissions, switching pulses (spikes) and perturbations in power supply. In our proposed method, the 4N35 model has been used for the feed back stage.

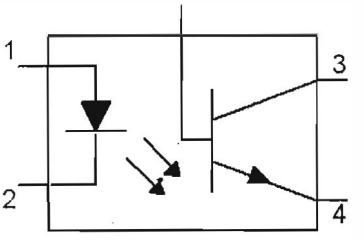


Fig 3.3.4(a) Optocoupler

An optocoupler contains a LED and a phototransistor, a barrier is provided between LED and phototransistor so that the transistor and the LED can be isolated. LED and the transistor are separated so that light may travel across a barrier but not the electrical current. When an electrical signal is applied to the input of the optocoupler, its LED lights, and its light sensor then activates, this light emission turns ON the phototransistor and a corresponding electrical signal is generated at the output.

With a photodiode as the detector, the output current is proportional to the amount of incident light supplied by the emitter. The diode can be used in a photovoltaic mode or a photoconductive mode.

In photovoltaic mode, the diode acts like a current source in parallel with a forward-biased diode. The output current and voltage are dependent on the load impedance and light intensity.

In photoconductive mode, the diode is connected to a supply voltage, and the magnitude of the current conducted is directly proportional to the intensity of light.

nlike a transformer, the optocoupler allows for DC coupling and generally provides gnificant protection from serious overvoltage conditions in one circuit affecting the other.

.4 Design Criteria

hc specification of the inverter is given below:

ower output	60 Watt
utput voltage	220 Volt A.C
put voltage	12 Volt D.C
requency	50 Hertz

.4.1 Design of the Driver Stage

.4.1.1 Driver circuit for N channel MOSFET

or method 1

o construct the driver circuit for N channel MOSFET, one 4148 diode, two PNP and one PN transistors have been used. To bias the MOSFET properly, R3 and R1 have been placed series which means a large portion of the supply voltage has been given at the gate of the OSFET. This is because it is known that, with increment of gate to source voltage, drain to urce voltage will be lower which means the drop across the MOSFET will be minimum. A fficiently large resistance R2 has been connected from the collector to base of PNP-1 to ndle large current. R4 has been used at the collector of PNP-1 to give the maximum ltage at the gate of the MOSFET [7].

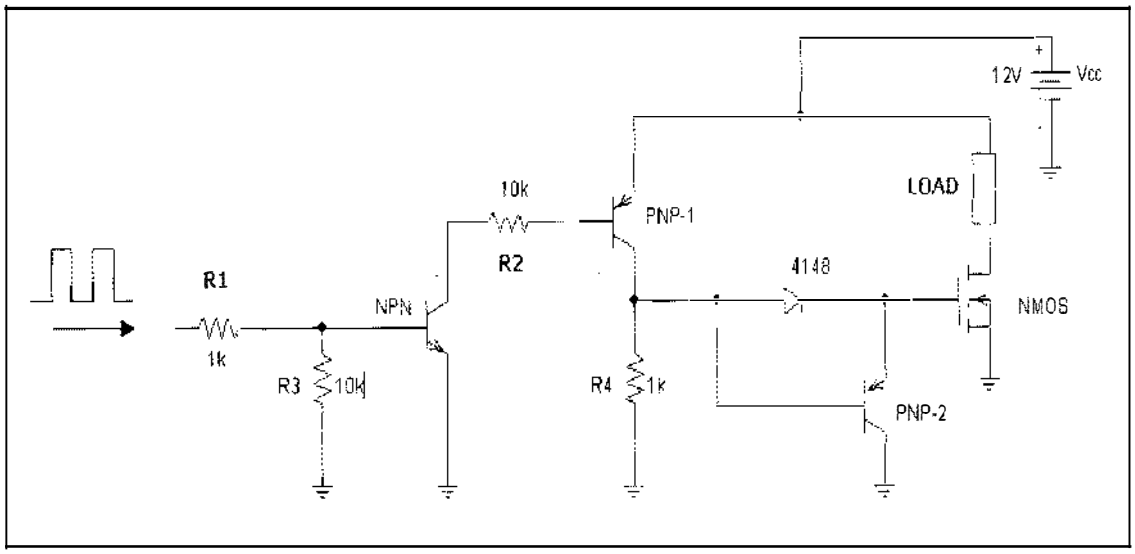


Fig 3.4.1.1(a) Schematic Diagram of N Channel MOSFET Driver for method 1

While the positive pulse appears the NPN turns ON which eventually turns ON the PNP- 1. As PNP-1 is turned ON, the power supply voltage appears at the gate of the MOSFET and turns it ON. The NPN transistor remains OFF while negative pulse appears. As a result the PNP-1 gets out of biasing condition. As the collector of the PNP-1 is connected to ground through a resistance so a negative voltage from ground appears at the gate of MOSFET which turns it OFF.

During the ON state time of MOSFET, a capacitance is formed due to the applied positive voltage to the gate which holds the voltage across it. At high frequency the MOSFET switches rapidly. Immediate after the positive pulse, when negative pulse appears the MOSFET does not turn OFF Instantly due to that capacitive effect which can be harmful for the device. To avoid that capacitive effect a PNP -2 transistor is used. This transistor is connected between the gate of the MOSFET and the ground. The base of PNP-2 is shorted to the collector of PNP-1. When the negative pulse appears immediate after the positive pulse, the PNP-2 gets ON and the storage charge that formed due the capacitance across the gate gets discharge instantly [7].

For method 2

For construction of the driver circuit for this method, two PNP and one NPN transistors have been used. R5 is chosen in such a way that during floating point, the negative through the R5 resistance turns the PNP ON and thus negative pulse reaches at the gate of the MOSFET which eventually turns it OFF.

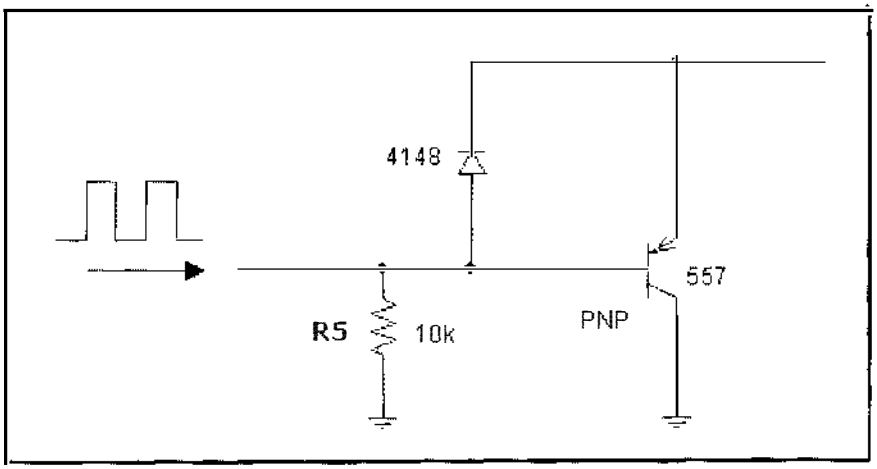


Fig 3.4.1.1(b) Schematic Diagram for N Channel MOSFET Driver for method 2

While positive pulse appears the diode gets forward biased and the pulses makes its way to the gate of MOSFET and turn it ON. Immediate after that stage during floating point, the negative through the R5 reaches at the base of PNP which turns it ON and thus a negative pulse appears at the MOSFET gate and turns it OFF.

3.4.1.2 Driver circuit for P channel MOSFET

To construct the driver circuit for P channel MOSFET, a 12 volts zener diode and an NMOS is needed. Actually, the NMOS controls the operation of PMOS here. R6 has been chosen in such a way to bias the NMOS properly. R7& and R8 has been connected in series. R7 usually a small value than R8 so that the NMOS can easily drive the PMOS. The zener diode has been placed in between supply voltage and gate of PMOS. It actually holds the 12 volt across it and maintains this voltage during supply voltage variation [12].

The principal application of the p-channel, enhancement mode POWER MOSFET is in switching power (or voltage) to grounded (ground return) loads. To drive the FET properly, the gate voltage must be referenced to its source. For enhancement-mode MOSFETs, this

gate potential is of the same polarity as the MOSFET's drain voltage. To turn on, the n-channel MOSFET requires a positive gate-source voltage, whereas the p-channel MOSFET requires a negative gate-source potential. During switching, a MOSFET's source voltage must remain fixed, as any variation will modulate the gate and thus adversely affect performance. The circuit diagram is given below:

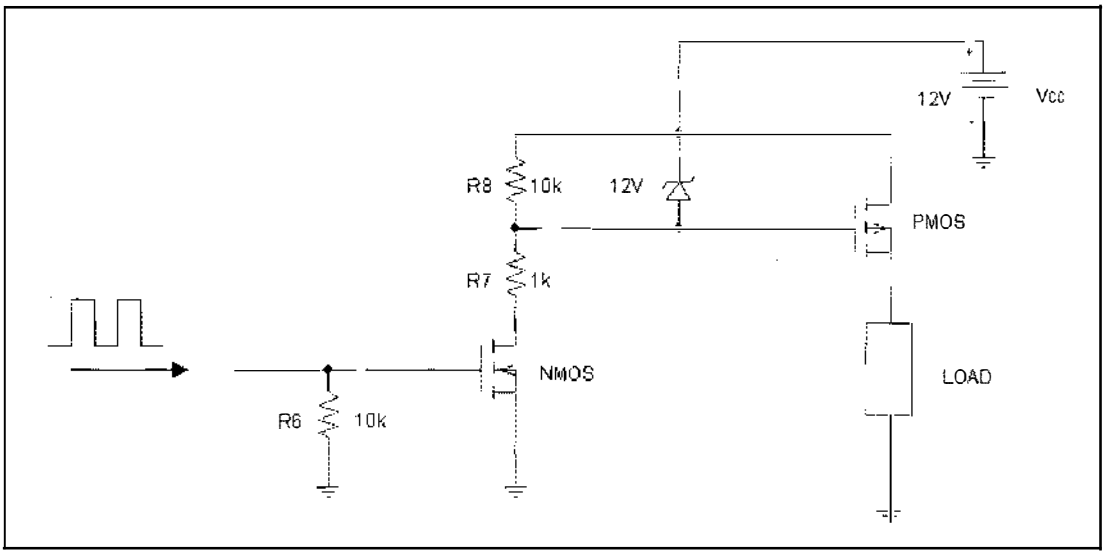


Fig 3.4.1.2(a) P Channel MOSFET Driver for method 1

From the above figure it is seen that the source of the NMOS is connected to the ground and the drain is connected to the gate of PMOS through a resistance. A resistance is connected from gate of the NMOS to ground. As the positive pulse occurs at the gate of NMOS it gets ON. For which a negative voltage appears to the gate of PMOS and turn it ON. When the negative pulse appears to the gate of NMOS it remains OFF, so the supply voltage comes across the gate of PMOS for which it remains OFF [12].

As method 2 has been selected for final hardware construction so the design of the driver stage is shown below in the figure:

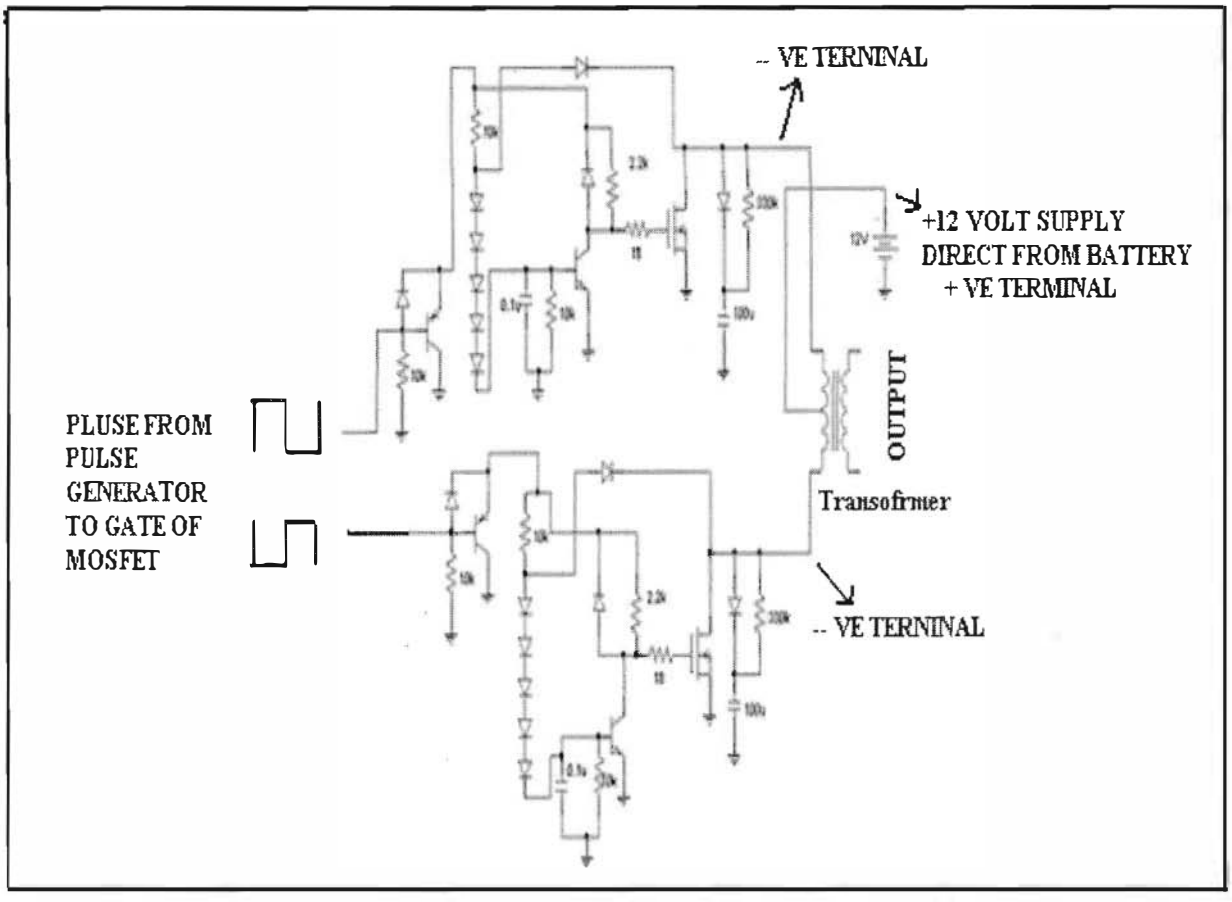


Fig 3.4.1.2(b) Schematic diagram of driver and power output stage

3.4.2 Design of the 50 Hz Antiphase Square wave Generator

The oscillator control frequency of the SG3524 and is programmed by RT and CT as shown in the figure:

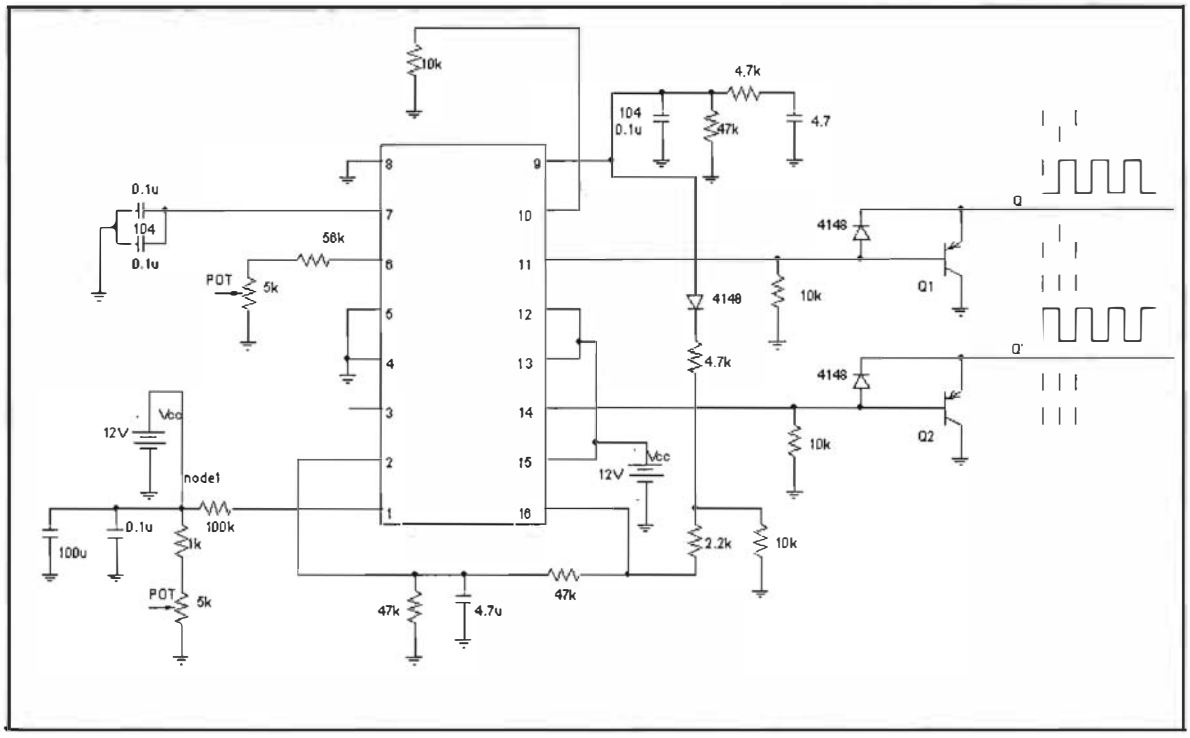


Fig 3.4.2(a) Schematic diagram of the frequency generator stage

Practical values of CT range from 0.001uF to 0.1uF. Practical values of RT range from 1.8k to 100k. This results in a frequency range from 130 Hz to 722 kHz.

As our motive is to supply a constant 50 Hz frequency from the pulse generator to the gate of the MOSFET for switching purpose, so we have chosen the value of RT and CT in such a way so that the frequency remains 50 Hz. The 50Hz generation process is described as following:

The collectors of two transistors are connected with Vcc. The 180 degree phase shifted outputs are taken from two emitters of the transistors. It is said in previous that a reference voltage is generated as power supply is concerned. Pin 7 and 6 generates the triangular wave signal. In pin 6 a resistor 56k is connected in series with a 5k variable POT. A stable 50Hz frequency can be obtained varying this POT. Pin 1 is used for adjusting duty cycle. A

resistance network is built in pin 1 as shown is the figure, two parallel capacitances are used in order to hold the terminal voltage. The supply voltage is divided in such a way that the maximum drop comes across the POT. Varying the POT duty cycle of the wave can be adjusted. Pin 9 is the output of comparator. The output of the comparator is connected to pin 16 with a resistance divider. Pin 16 is a reference voltage that is generated applying power supply. Now this voltage is divided with two 4.7k resistances and feedback to pin 2. Another 47uF capacitance is used to hold that terminal voltage. Pulse width would vary if the 5k POT get varied. Any change pin 1 voltage varies the POT fixes the pulse width.

3.4.3 Design of the power output stage

The power rating is 60 watts and the output voltage is 220 volts.

Let the load is resistive, so the load current

$$I2 = \frac{60}{220} = 0.2727 \text{ A}$$

Let the transformer primary voltage is 12-0-12 volt and transformation ratio is

$$a = \frac{V1}{V2} = \frac{12}{220} = 0.0545$$

The corresponding primary current

$$I1 = \frac{I2}{a} = \frac{0.2727}{0.0545} = 5.004\text{A} = 5\text{A}$$

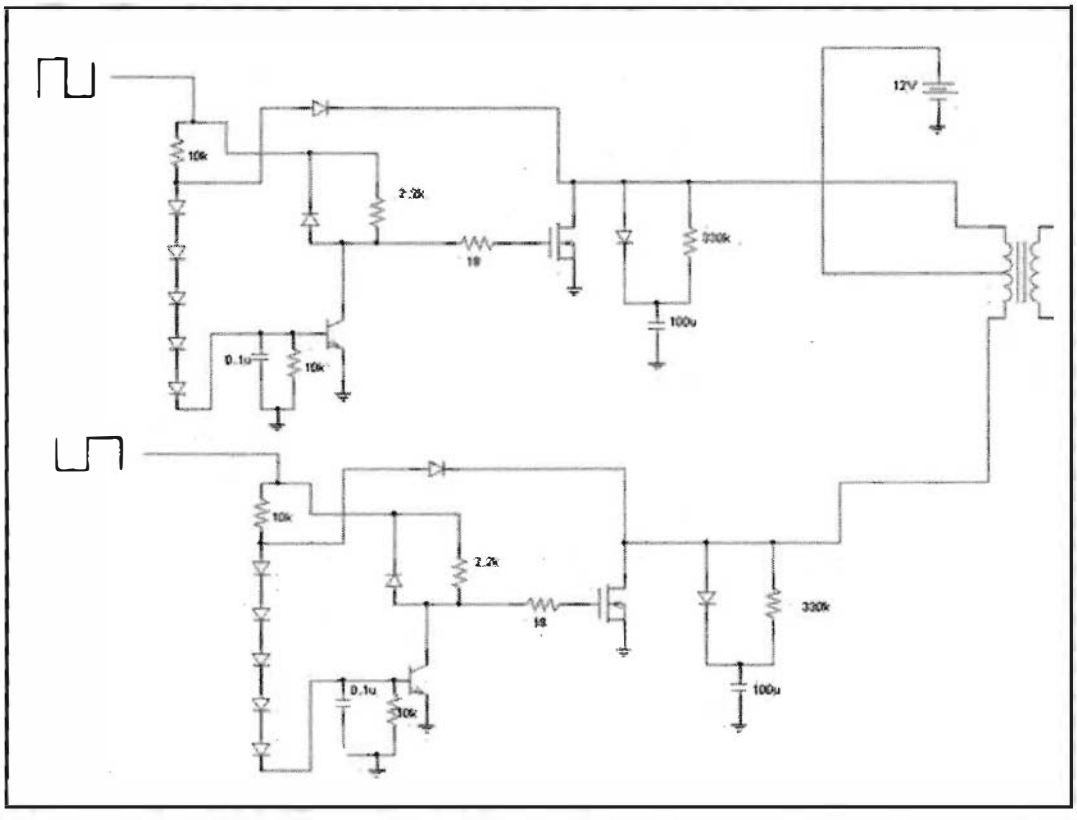


Fig 3.4.3(a) Schematic diagram of the power output stage

A semiconductor switching device is needed which is able to carry this 5A current. IRFZ44 nd *IRF9520 are the suitable devices for that. The ratings of these devices are discussed in* revious sub-sections. The connections of these devices have been shown in the above figure. low, as 5A current is flowing through the drain of the MOSFET. So, from the equation of rain current (in linear region),

$$I_d \text{ (linear)} = \mu \, C_{ox} \frac{W}{L} \times \{(V_{gs}-V_t) V_{ds}\} - \frac{V^2}{2} \quad \ldots\ldots\ldots \text{(xiii)}$$

rom the above equation, assuming the value of Vds small as the switching loss is very low ccording to our design. Then the square term can be neglected. Now, taking a constant value f conduction parameter, threshold voltage, the value of Vgs can be obtained which is ufficiently a large value.

he square wave generator stage is not able to carry this amount of voltage. So, multiple tage amplification is required.

3.4.4 Total Harmonic Distortion (THD) analysis

The equation of total harmonic distortion is given below:

$$THDv = \frac{\sqrt{\sum_{n=2}^{\infty}(V_{RMS})^2 - (V_{1,RMS})^2}}{V_{1,RMS}} \quad \text{..... (xiv)}$$

From the simulation the fundamental peak is obtained approximately 10.80V for first method. And for second method it is about 9 V.

Therefore, THD for the first method is $= \frac{(V_s^2 - V_{1rms}^2)^{0.5}}{V_{1rms}^2}$

$= 0.4843$

$= 48.43\%$

THD for the second method is $= \frac{(V_s^2 - V_{1rms}^2)^{0.5}}{V_{1rms}^2}$

$= 0.8819$

$= 88.19\%$

So the above calculation states that method 1 gives a better THD response. Huge amount of harmonics occurs for second method. It can be said that, there'll be less harmonic distortion for method 1.

3.4.5 Selection of the output Transformer

In this project we have used a 12-0-12 transformer. Which means it is a center tapped transformer with three phase input. And it has current ratings of 6A.

In this section a brief discussion is done regarding transformer. This section highlights the improvement that can be done to design a transformer. This will result a decent construction of a single phase inverter. A transformer will provide best characteristics when the primary coil that takes over magnetization of the iron core fits closely around the core [2]. In this project transformer would be the 220 Volts coil, on our inverter however it will be the 12 volt coil.

The main objective is to choose the number of turns so that the desired voltage could generate.

For the computation of the numbers of turns the following consideration applies:

Computation

We specify the maximum magnetic induction on a value of 1.5 Tesla [2]. For computation now only two simple equations are necessary:

1. $U_{ind} = n \times F / t$ ..... (xv)

   $n = U_{ind} \times t/F$

2. $F = B \times A$ ..... (xvi)

U_{ind}=induced voltage n=number of turns

F = magnetic flux t=transistor switch-on time

B= magnetic induction A=cross-section area of transformer core

For power electronics resistive load shall not calculate on energy conversion. Thus the whole battery voltage will apply on the transformer coil for the whole switch-on time of the transistor. The switch-on time results in 5 milliseconds; depended on the period of the 50

cycles / second oscillation and a duty-cycle of 25% (period of a 50 cycle oscillation is 1 / 50 Hz = 20 milliseconds).

These calculations are done for 60 VA transformers.

At low frequency such as 50-120Hz should use laminated core

Let the cross-section area of the transformer calculates to A = 60 mm x 80 mm = 4,8 x 10^{-3} m^2 [2].

U_{ind} = 12 Volt B= 1.5 Tesla = 1.5 Vs/ m^2

$t = 5\ ms$ $A = 4.8 \times 10^{-3}\ m^2$

With equation 2 magnetic flux calculates to F = B x A = 1.5 Vs/ m^2 x 4.8 x 10^{-3} m^2 = 7.2 x 10^{-3} Vs

Now the value of F is being set in equation 1.

Number of turns on primary $N_P = U_{ind}$ x t/F = 12 V x 5 x 10^{-3} s / (7.2 x 10^{-3} Vs) = 8.33 (rounded up 9 turns).

Number of turns on secondary $N_S = U_{ind}$ x t/F = 220V x 5 x 10^{-3} s / (7.2 x 10^{-3} Vs) = 152.78 (rounded up 153 turns).

.4.6 Design of the Feed Back Stage

he circuit for feedback stage is given below:

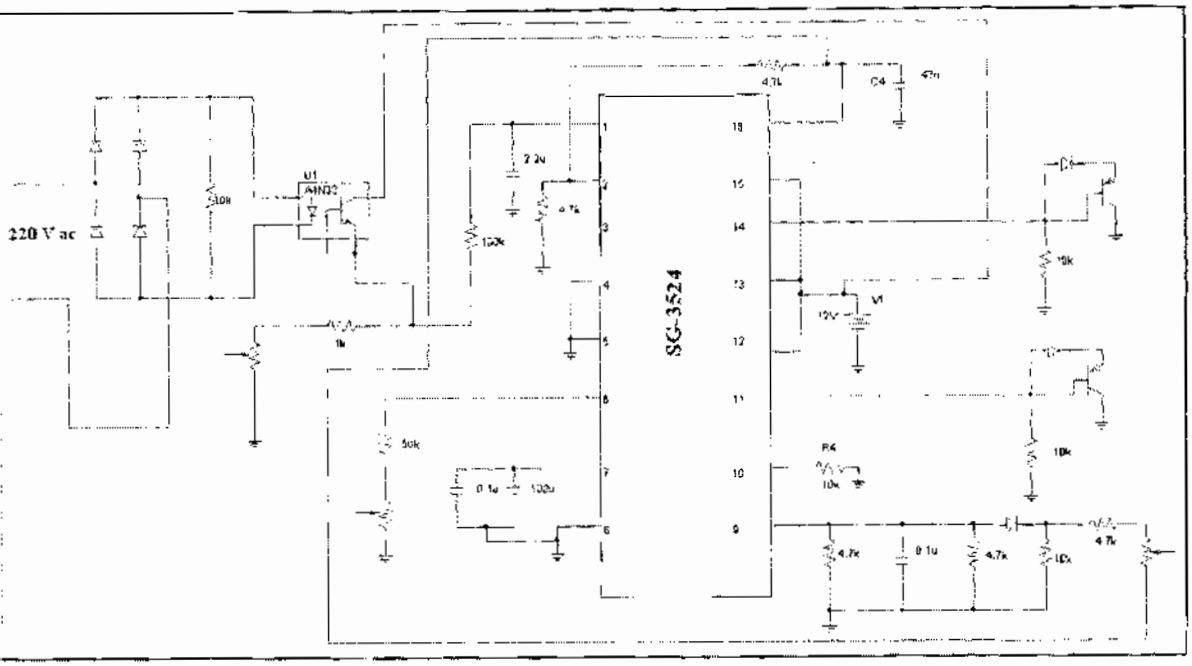


Fig 3.4.6: Figure of feedback stage

bove figure is proposed for feedback output stage. In this project the feedback stage is not onstructed practically. This is a proposal that can be applied as a feedback stage.

eedback circuit contains an optocoupler. The voltage that is obtained to the output is eedback to the comparator of SG-3524 through optocoupler. Optocoupler isolates the pulse eneration circuit, apart from high side. 220V output voltage passed through a full bridge. So unidirectional AC voltage can be obtained. If AC voltage is applied to the optocoupler nput, then the diode within the optocoupler remains forward bias only for half cycle. It will emain OFF for the negative cycle. That's why a bridge is used here. When the corresponding urrent of 220v goes from the internal diode of optocoupler, it induces a minimum voltage rop of 0.7V across it and generates a light. This lighting turns on the photo transistor, which nakes the collector and emitter short. The collector was biased with the supply voltage. Therefore supply voltage goes to the resistance divider terminal as shown in above figure, nd the pulse width get adjusted by the POT in order to generate anti phase 50Hz square as escribed in previous section.

Construction and Testing

.1 Construction

e different block designs discussed previously in this chapter were constructed in Vero
rd. Each block after construction was tested individually.

.2 Testing

e following tests are made for calculating the performance of designed inverter.

.2.1 Output Wave shape of Square wave Generator

cording to the design, the output should be two antiphase square waves of 50 Hz, having
volt peak.

e photograph is shown below, is taken from an oscilloscope screen, when the oscilloscope
onnected to the output of the stage.

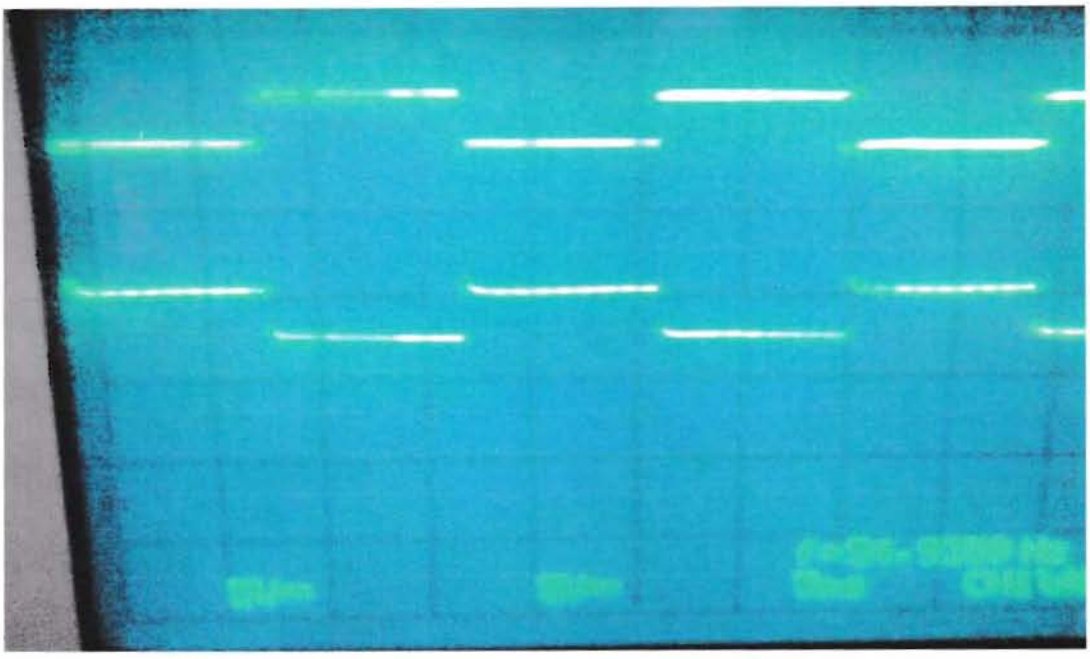


Fig 3.5.2.1(a) Square Wave Generation from SG3524

.2.2 Voltage Wave shapes of transformer Primary

· method 1

Primary voltage wave shape at no load

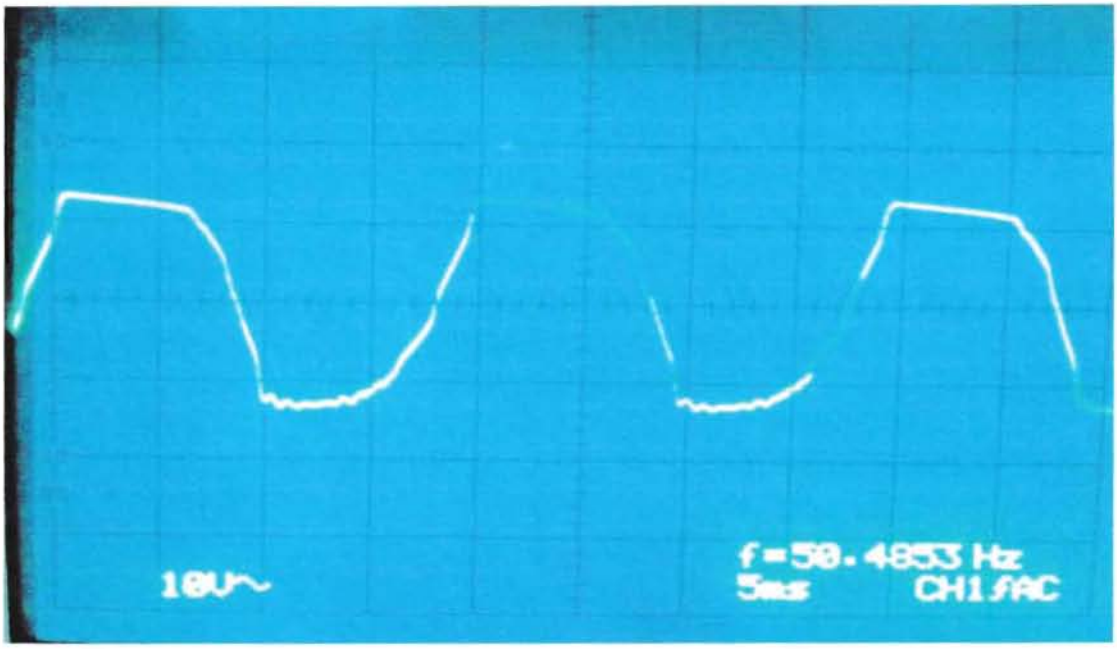


Fig 3.5.2.2(a)

For method 2

The voltage wave shapes of transformer primary and secondary are shown below

(b) Primary voltage wave shape at no load

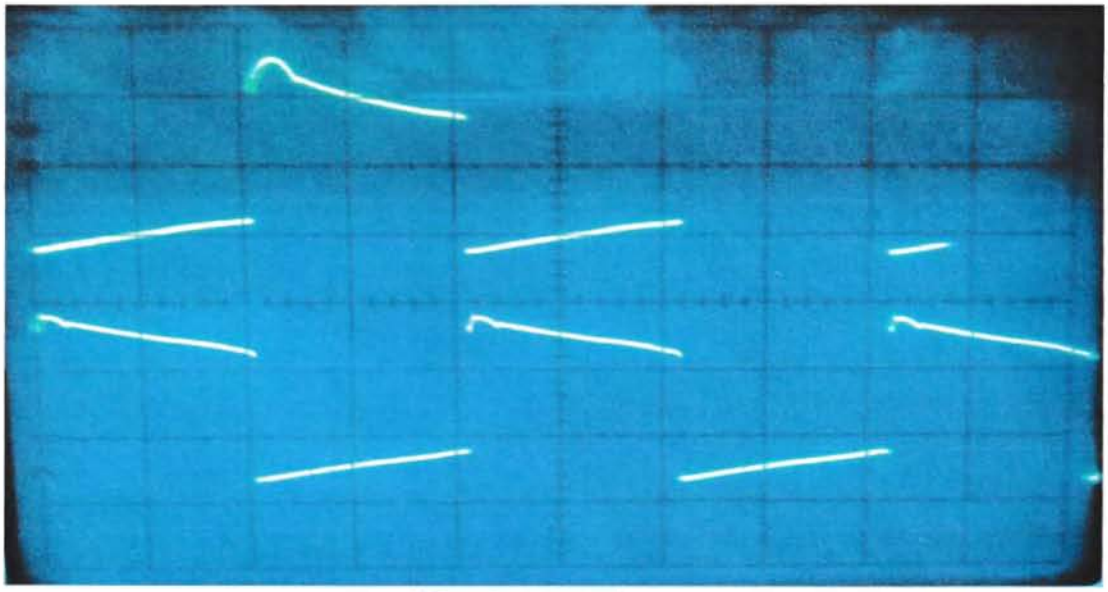


Fig 3.5.2.2(b)

(c) Secondary voltage wave shape at 60W load

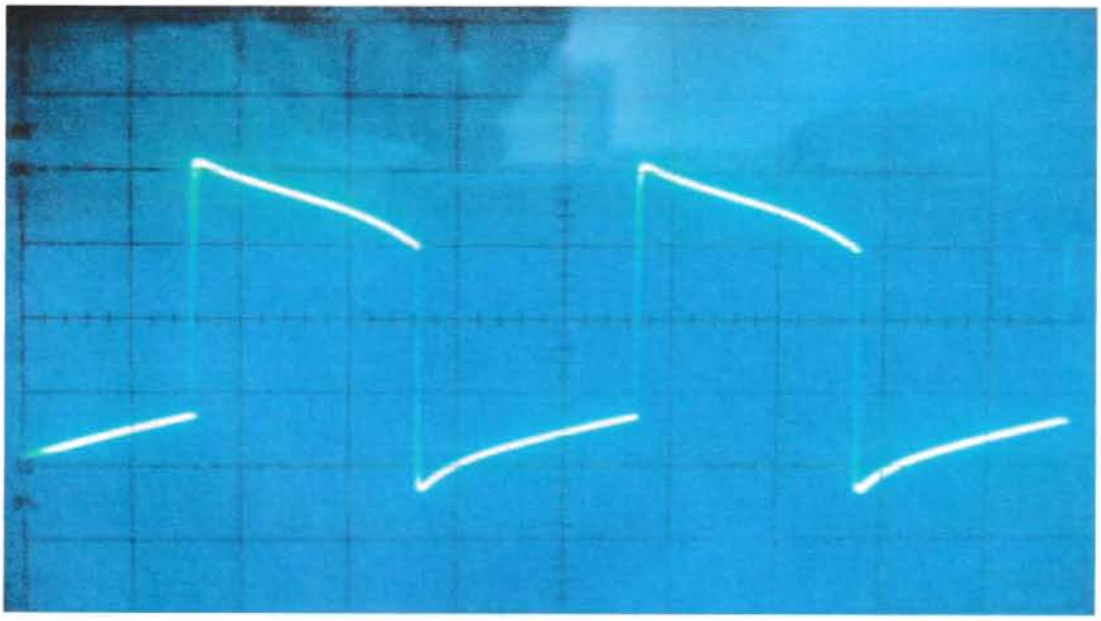


Fig 3.5.2.2(c)

3.5.2.3 Constructed Single Phase Inverter

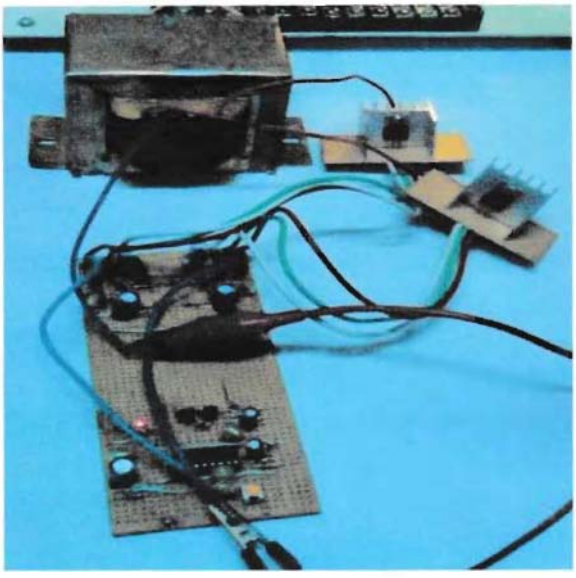


Fig 3.5.2.3(a) Inverter Hardware

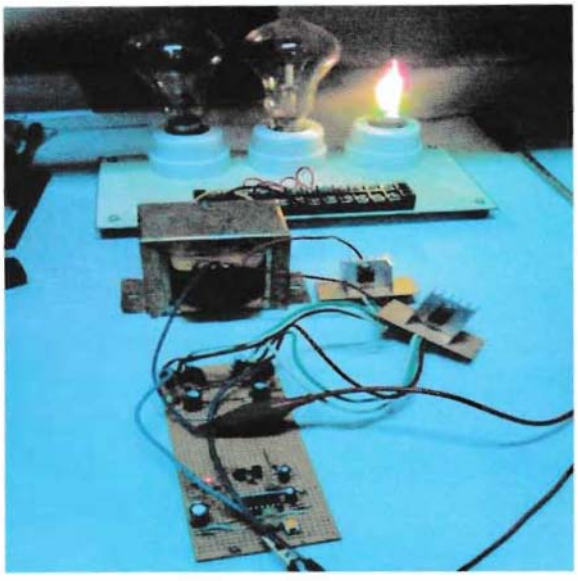


Fig 3.5.2.3(b) Inverter with 5W load

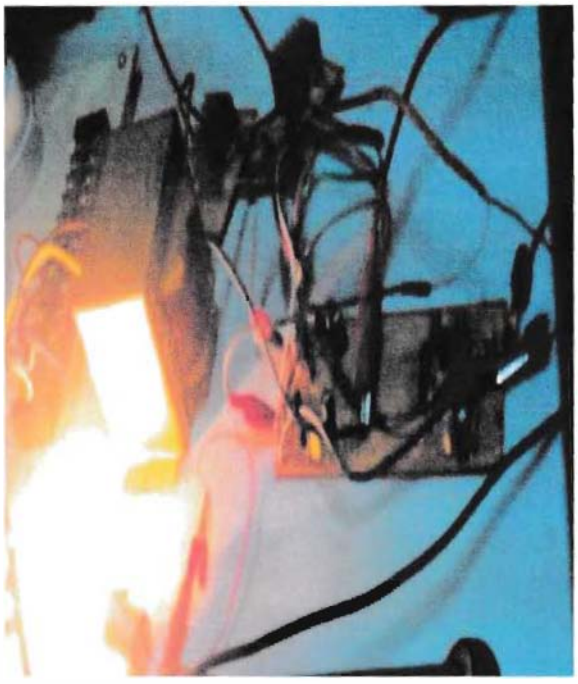


Fig 3.5.2.3(c) With 60 watt load

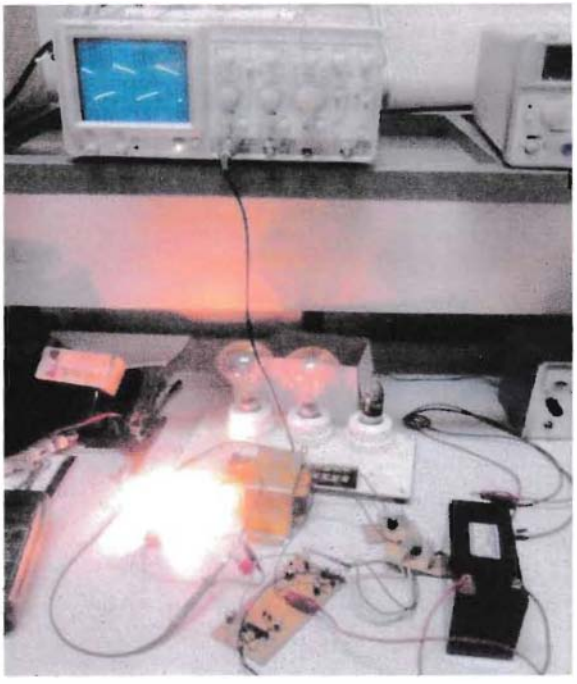


Fig 3.5.2.3(d) Wave shape at 60W load

n the above table, it can be observed that the experimental values are more or less similar
ıe theoretically calculated values. Due to some internal losses in the transformer coils and
r parameters like diodes, transistors, the obtained output power differ a little than the
red quantity which is in suitable range.

Conclusion

inverter was constructed and tested and found to work satisfactory with operating input
age of 12V. The output voltage of this inverter is almost constant at given load. The
erimental input and output wave shapes matches the computer simulated wave shapes.

CHAPTER 4
TECHNIQUE OF IMPROVEMENT IN EFFICIENCY

4.1 Introduction

Efficiency, literally, means the capability of a specific application of effort to produce a desired outcome by wasting the minimum amount of effort. In engineering terms, it can be said that efficiency is the ratio of a machine's energy output to the energy input.

For an inverter, we can say that efficiency is the percentage of power that goes into the inverter and comes out as useable AC current. In our proposed project, we emphasized more on the inverter efficiency. Our effort was to reduce the internal loss of the circuit of the inverter and get the maximum output power.

4.2 Proposed Technique for Improved Efficiency

The operation of our proposed inverter is mainly based on the switching of MOSFETs. In a conventional inverter built nowadays, the switching is done using only N-type MOSFETs. The reason of using NMOS is that it gets less heated while switching. But on the other hand the efficiency is being compromised using only NMOS. This is because we experimented our proposed inverter using only NMOS and found that during positive switching, NMOS does not function properly. There is a noticeable voltage drop, i.e. around 3V across the NMOS. As a result, the desired output was not obtained at no load. Due this significant drop across NMOS at high side, full conduction is not possible at no load output and thus the internal loss increases and the output power is not as desired. Thus in our proposed inverter, we have implemented two methods.

For method 1

In our proposed inverter, we used PMOS for the positive or high side switching and NMOS for the negative or low side switching. The advantage of using PMOS in high side switching is that the voltage drop across the PMOS while switching is very low i.e. 0.3V compared to the NMOS's 3V. Also, using NMOS for low side switching gives us a smooth conduction with a very less voltage drop. As a result, using this arrangement, we were successful at reducing the internal loss of the inverter and get almost full conduction from the MOSFETs.

For method 2

In this method, we used no switching in the positive or high side. The supply voltage from the battery had been directly connected to the one terminal of the transformer. As a result, there was no switching loss at the positive or high side. Besides, using NMOS in negative side provides smooth conduction due to the high mobility of electrons in it. So, this arrangement was more beneficial to reduce internal loss and increase efficiency.

After experimenting both the methods, it was observed that method 2 was much better than method 1 in terms of efficiency. Besides, some complexities were also observed in method 1 during positive switching. So, after experimentation, method 2 was found to be a better one and had been finalized for the final hardware construction.

4.3 Implementation and Outcome

Method 1

At no load, we achieved the output voltage of 10.63V by giving an input of 12V. So, by using PMOS for high side switching and using NMOS for low side switching, we were able to increase the inverter efficiency.

$$\text{Efficiency} = \frac{output\ voltage}{input\ voltage}\ X\ 100\ \%$$

$$= \frac{11.3}{12} \text{ X } 100\%$$

$$= 94.17\ \%$$

Method 2

At no load, we achieved the output voltage of 11.6V by giving a 12V input. So, by switching only the negative side and connecting the positive side directly to the transformer, we were able to achieve an even better efficiency compared to the previous method.

$$\text{Efficiency} = \frac{output\ voltage}{input\ voltage}\ X\ 100\ \%$$

$$= \frac{11.6}{12} \text{ X } 100$$

$$= 96.67\ \%$$

From the above two calculation it is obvious that method 2 has much better efficiency than method 1. So, it can be said that the experiment for improving efficiency by reducing internal loss was a success

.

4.4 Conclusion

One of the prior concerns during construction of the inverter was the efficiency. That is why, two methods were put into operation and the better solution in terms of efficiency was finally constructed. The notion was to improve the efficiency by reducing the internal switching loss.

CHAPTER 5
SUMMARY, CONCLUSION AND RECOMMENDATIONS

1 Summary

single phase inverter under fixed output voltage is designed and constructed in this project. chapter-1, introductory discussion, proposed method and scope of the project is discussed. nciple of operation, modulation technique is discussed and computer analysis is done in apter-2. In Chapter 3, details design procedure; construction and testing are discussed and died. Chapter 4 includes discussion on efficiency and the techniques to improve it.

2 Conclusion

e output voltage of this single phase inverter is square wave. The square wave sometimes kes problems in reactive circuits. It restrains several harmonics, which causes heating. But the important benefits of square wave are that its peak value is constant with respect to ne. To operate a transistor at a definite voltage, the square wave does not take any time ereas the sine wave takes some time for the transition to the peak.

e output voltage of the inverter is constant up to the designed load. When the battery is ar to discharge level the output voltage does not remain constant. By the proper design of a nsformer and by the use of a fully charged battery this problem can be solved.

3 Suggestions for Future Work

e inverter that is constructed for this project is for fixed load. Our suggestion is to design s inverter for variable loads, by introducing a feedback network. Another important aspect harmonic distortion. The design would be more efficient, if harmonics effect is reduced m the output. Single phase inverter with advanced PWM can be further studied.

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