Effect of Non-Uniform Doping on Gate C-V Characteristics of MOSFETS

By

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Dedicated
To Almighty Allah
Who schedules everything,
To leader of humankind
Nabi Muhammed (sallallaahu alaihi wa sallam)
And To Our Parents
Who gave us Life.....

Abstract

The goal of this thesis is to determine the effects that the actual physical structure of a metal-oxide-semiconductor (MOS) capacitor. A semi-classical numerical model is presented to investigate the effect of non-uniform substrate doping on gate C-V characteristics of MOSFETs. Poisson's equation is solved numerically neglecting quantum mechanical effects. Maximum surface potential is considered as equal to $2\phi_F$. Calculated gate C-V characteristic for step doping profile and Gaussian doping profile are compared with C-V for uniformly doped substrates. It is observed that non-uniform doping has great influence in C-V characteristics of MOSFETs in weak accumulation and depletion regime. It also affects the threshold voltage.

Acknowledgment

We would like to first thanks to Allah, who gave us the strength through the year completing my graduation and our parents for giving their constant support. After that we would like to express our sincerest thanks to Professor Anisul Haque, Chairperson of Electrical & Electronic Engineering, East West University, Dhaka, for his guiding, technical insight and supporting us throughout this project. He also has been an exceptional role model of life. It has been memorable that he encouraged and supported us while we were in deep depression.

AUTHORIZATION PAGE

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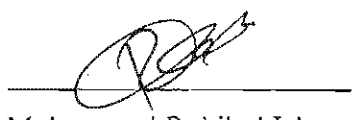

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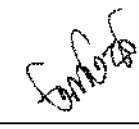

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Chapter 1

Introduction

MOSFET is by far the most popular and common Field Effect Transistor after the invention of it in 1925 by Julius Edger Lilienfeld. According to Moore's Law the number of transistors per chip will get doubled in each year [1]. But the size of the chip can not increase with the same proportion. In order to be space convenient the chip size should be small as well. That is why scaling down the size of the MOS transistor is of great importance. The critical elements in device scaling are the gate dielectric thickness, the gate length and the substrate doping density [2]. As sizes are shrinking down doping density plays a vital role for MOS transistor operation [3].

1.1 Background of the Topic

The MOS capacitor consists of a metal-oxide-semiconductor layer structure which forms a voltage dependent capacitor. This particular structure has been studied extensively because it is present in all MOS transistors. The real importance of C-V curve is that a large number of device parameters can be extracted from the curve [4]. Its analysis provides details related to the threshold voltage of the MOS transistor and the quality of the oxide-semiconductor interface. In addition it is frequently used to measure device parameters such as substrate doping concentration, oxide thickness and oxide charge. These parameters can provide critical device and process information.

The capacitance of a MOS structure is voltage dependent since the semiconductor region under the oxide can be either depleted of carriers, can accumulate carriers or an inversion layer can be formed. For instance in a p-type substrate one finds that for a large negative

voltage, V_{GB} applied to the gate, holes are attracted to the interface, causing accumulation. A positive voltage on the other hand repels the holes which are present in the p-type material and thereby creates a depletion layer. A larger positive voltage at the gate causes sufficient bending of the energy bands in the semiconductor at the interface so that "inversion" occurs. An even larger positive voltage causes "strong inversion" where the carrier density at the oxide-semiconductor interface exceeds that of the opposite carrier type in the substrate [5]. The capacitance of the structure changes accordingly, but before any discussion about the capacitance can be started, one has to distinguish between "low frequency" and "high frequency" capacitance measurements. The low frequency capacitance is measured when the semiconductor is in thermal equilibrium at any time while the voltage is applied [5]. This type of measurement is also called the quasi-static capacitance measurement. For a high frequency capacitance measurement, one uses a frequency which is so high that the minority carrier concentration can not follow the applied AC voltage and therefore maintains its value as determined by the DC bias voltage. The high frequency capacitance is obtained from the magnitude of the AC current that is out of phase with the applied voltage. Both capacitance measurements are performed as a function of the bias voltage which is slowly swept from accumulation, through depletion into inversion. For simplicity of analysis all other parameters are considered as ideal in measurement of C-V characteristic. But in practical cases MOS transistor has few nonidealities. Three main nonidealities may be included: at the interface, in the gate material, and in the semiconductor. In the semiconductor, doping density is considered as uniform. Present day CMOS process use ion implantation to adjust the threshold voltage. The substrate doping in the transistor can thus no longer be considered as uniform. Step, retrograde, Gaussian and constant gradient doping profiles are common non-uniform profiles. The non-uniform doping mainly affects the relation between the depletion charge and channel voltage [6].

1.2 A glimpse of previous works on MOSFETs with non-uniform substrate doping

Lallement and others derived the solution for non-uniform substrate doping [6]. They presented five different type non-uniform doping and derived equation for depletion charge and threshold voltage.

A numerical calculation of ideal C-V characteristics of non-uniformly doped MOS capacitor was carried out by Sissi and Cobbold [7]. In this paper they also solved Poisson's equation but for boundary condition they considered surface potential. They chose several surface potential and for respective surface potential gate voltage was calculated.

Simonetti and others observed the effect of substrate doping profile on C-V curve for MOS capacitor [8]. They simulated with some Gaussian doping profile and presented their results including quantum effect. They also provided the effect of different oxide thickness. But they did not provide the full C-V characteristics as only accumulation region was simulated.

1.3 Objective of the work

The C-V curve gives direct information about the penetration of the field in the semiconductor (minimum in accumulation, maximum in depletion, etc.) and about the varying charges (majority and/or minority carriers) allowing a direct assessment of the field effect. C-V characteristics are widely used to characterize the semiconductor, oxide, and Si-SiO_2 interface [9] [10]. Test capacitors are customarily measured to monitor process lines, and a vast literature exists concerning the MOS capacitor as a technology characterization tool (see, for example, references in [10]). For technology characterization purposes, the inclusion of accurate models of the different non-idealities is paramount. To develop compact models of the MOS transistor we must keep the capacitive model as simple as possible. That is why C-V behavior seems a powerful diagnostic tool for device manufacturer. One can identify deviations from ideal in both

oxide and semiconductor parameters. So, accurate C-V measurement for practical MOS structure is routinely monitored. Doping profile has a significant influence in C-V behavior. Considering doping profile as uniform will not reproduce the appropriate C-V behavior for practical MOS structure. We tried to focus the changes in C-V behavior for different non-uniform doping profile. Poisson's equation is solved numerically neglecting quantum mechanical effects. Maximum surface potential is considered as equal to $2\phi_F$. No weak accumulation regime considered in calculation.

1.4 Thesis outline

In this report, we represented our work in a few chapters. These chapters are as follows:

- **Chapter 2:** In this chapter, the physics and operation of MOS devices are discussed in detail. Particularly, the theory of MOS capacitor is presented. The dependency of MOS capacitance on frequency and applied voltage is also shown. Presentations of various equations on MOS capacitor are described with proper description and figure.

- **Chapter 3:** The proposed model with vertically non-uniform substrate doping for MOSFETs is explained in detail in this chapter. The equations of the model along with compact mathematical analysis and plots of electric field profile curves for an arbitrary non-uniform doping profile is presented. The way to identify maximum depletion width and by this calculation of different charges and generation of C-V characteristics are explained in this chapter.

- **Chapter 4:** Two realistic non-uniform doping profiles (Step doping profile & Gaussian doping profile), used for simulation and generation of C-V characteristics of MOSFETs, are shown here. We highlighted the deviations from ideal C-V characteristic with uniform doping profile by suitable plots.

- **Chapter 5:** Summary of our work and suggestion for future works are made in this chapter.

Chapter 2

MOS Capacitor Physics and Operations

2.1 MOS Basics

To understand the MOSFET, it is convenient to analyze the MOS capacitor first, which constitutes the important gate-channel-substrate structure of the MOSFETs. The MOS capacitor is a two terminal semiconductor device of practical interest in its own right. As indicated in figure 2.1, it consists of a metal contact separated from the semiconductor substrate by dielectric insulator. Almost universally, the MOS structure utilizes doped silicon as the substrate and its native oxide, SiO_2, as the insulator. In the silicon-silicon dioxide system, the density of surface states at the oxide semiconductor interface is very low compared to the typical channel carrier density in a MOSFET. Also, the insulating quality of the oxide is quite good [11].

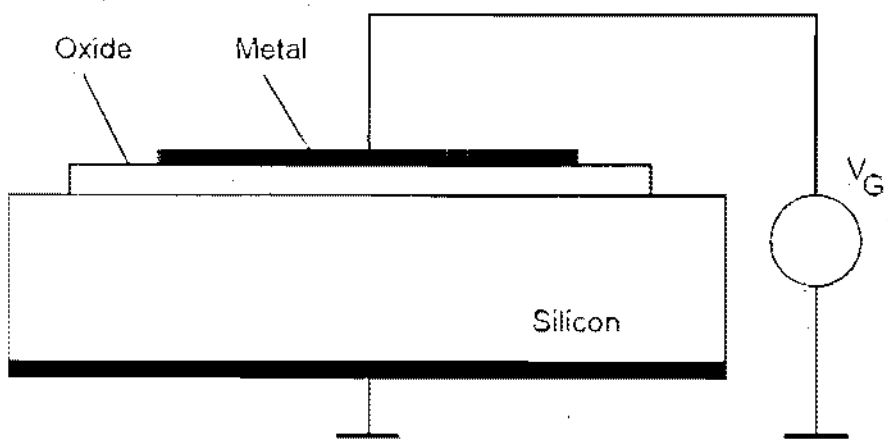

Fig 2.1 Schematic diagram of a MOS capacitor

MOS capacitor consists of: Metal with work function ϕ_M, Oxide is SiO_2 also known as Silica and the semiconductor is Si. Work function of semiconductor is ϕ_S. Here we consider p-type Si substrate. Initially we assume that $\phi_M = \phi_S$. In figure 2.2 E_{VAC} is the vacuum level.

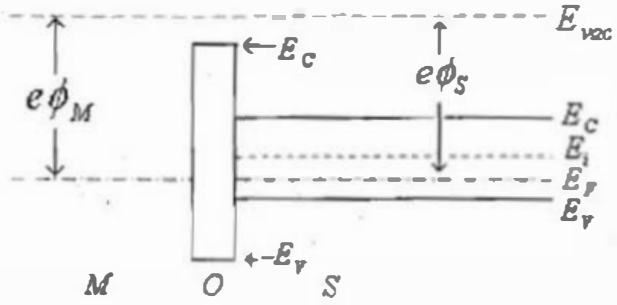

Fig. 2.2 Band diagram of MOS capacitor in equilibrium

Depending on the applied voltage on the gate three regions can be created; these are Accumulation, Depletion and Inversion.

Accumulation

If gate voltage (V_G) is less than flat band voltage (V_{FB}) accumulation starts. For this negative charge in the gate holes or positive charge in silicon surface will be attracted from the semiconductor. Thus the holes will be accumulated in the surface.

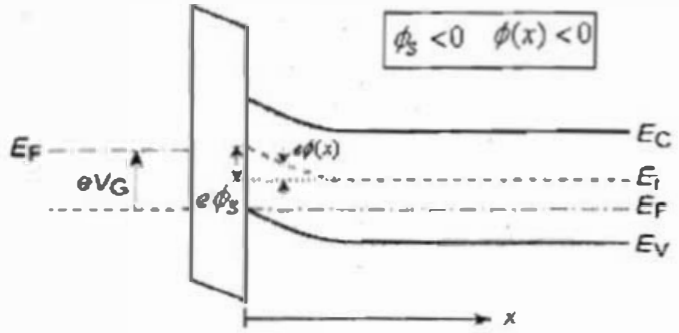

Fig. 2.3 Band diagram of MOS capacitor in accumulation

Depletion

If we increase V_G above V_{FB}, the total charge on the gate will become more positive. In this case the positive charge in the gate will simply deplete the positive charge of semiconductor and leaving it depleted. This stage is called depletion. Here W_D is called depletion width.

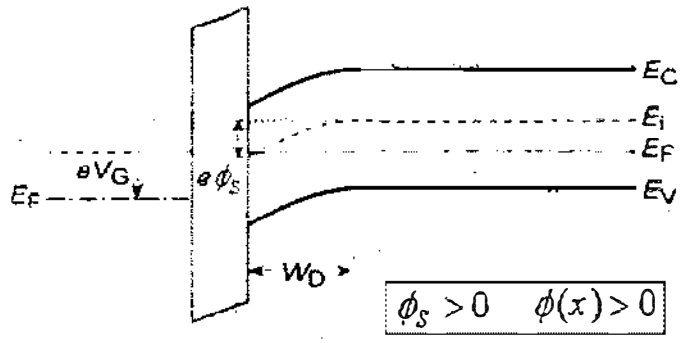

Fig. 2.4 Band diagram of MOS capacitor in depletion

Inversion

As V_G is increased further, surface potential will become sufficiently positive to attract the free electron in the surface. This stage is named inversion.

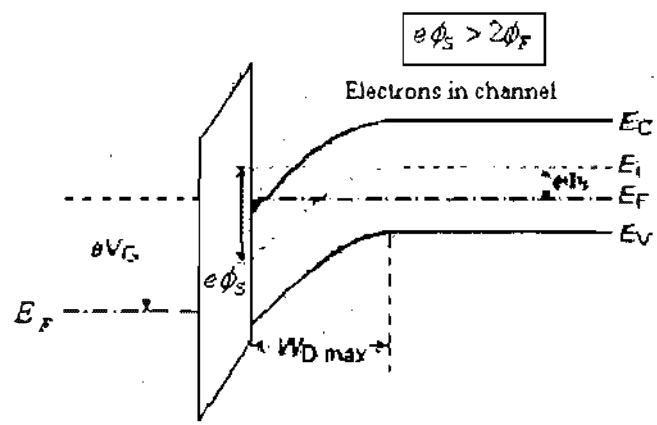

Fig. 2.5 Band diagram of MOS capacitor in inversion

The voltage at which inversion starts is called threshold voltage. For this voltage, concentration of holes and concentration of electron are equal at the surface.

2.2 Space Charge Density vs. Surface Potential

The electron and the hole concentrations are related to the potential $\phi_S(x)$. The equilibrium electron concentration is defined as [12]

$$n_0 = n_i e^{(E_F - E_i)/KT} \tag{2.1}$$

(Here n_i is the intrinsic electron concentration; E_F is Fermi level; $q\phi_F$ is the position of Fermi level above the intrinsic level E_i for the semiconductor; K is Boltzmann Constant; T is temperature in Kelvin).

From this we can relate the electron concentration at any x to this value [12],

$$n = n_i e^{-q(\phi_f - \phi)/KT} = n_0 e^{q\phi/KT} \tag{2.2}$$

Similar thing happens for holes,

$$p_0 = n_i e^{q\phi/KT} \tag{2.3}$$

$$p = p_0 e^{-q\phi/KT} \tag{2.4}$$

At any x value we can combine these equations with Poisson's equation (2.5) and the usual charge density expression (2.6) to solve for $\phi(x)$ [12]

$$\frac{\partial^2 \phi}{\partial x^2} = \frac{-\rho(x)}{\varepsilon_S} \tag{2.5}$$

Where ε_S is the semiconductor permittivity, and the space charge density $\rho(x)$ is given by [12, 13]

$$\rho(x) = q(N_d^+ - N_a^- + p - n) \tag{2.6}$$

One thing to note here deep inside the semiconductor, we have $\phi(\infty) = 0$. For any gate voltage (V_G) an electric field profile $F(x)$ and corresponding potential profile $\phi(x)$ will be present in semiconductor. We should keep in mind that $F = -\frac{d\phi}{dx}$. The following expression can be derived for the electric field F_S at the insulator–semiconductor interface, in terms of the surface potential

$$F_S = \sqrt{2}\frac{KT}{qL_{DP}} f(\frac{q\phi_S}{KT}) \qquad 2.7$$

Where the function f is defined by

$$f(u) = \pm\sqrt{[\exp(-u) + u - 1] + \frac{n_{po}}{N_a}[\exp(u) - u - 1]} \qquad 2.8$$

Where, n_{po} is the minority carrier concentration in substrate.

And

$$L_{DP} = \sqrt{\frac{\varepsilon_S KT}{q^2 N_a}} \qquad 2.9$$

Here L_{DP} is called the Debye length [12]. Debye length is the distance over which significant charge separation can occur.

Using Gauss's law, we can relate the total charge Q_S per unit area in the semiconductor to the surface electric field by [12]

$$Q_S = -\varepsilon_S F_S \qquad 2.10$$

Or the equation is

$$Q_S = \sqrt{2\varepsilon KTN_A[(e^{-q\phi_S/KT} + \frac{q\phi_s}{KT} - 1) + \frac{n_i^2}{N_A^2}(e^{q\phi_S/KT} - \frac{q\phi_S}{KT} - 1)]} \qquad 2.11$$

Here again the electric field deep in the substrate is zero.

The space charge density per unit area Q_S in equation (2.11) is plotted as a function of the surface potential ϕ_S in the figure (2.6) below. As the surface potential is negative (accumulation), it attracts and forms an accumulation layer with the help of majority carrier holes at the surface. Here the first term in equation (2.11) became dominant, and the accumulation space charge increases very strongly (exponentially) with negative surface potential. It is easy to see why by looking at equation (2.3 & 2.4), which gives the surface hole concentration in a p-type semiconductor as a function of depth.

When the gate is at positive voltage, equation (2.11)'s second term become the dominant one. Even though the exponential term is quite large, when multiplied by the ratio of the minority to majority concentration, it is initially negligible. Hence the space charge for small positive surface potential increases as ~ $\sqrt{Ø_s}$ as shown in the figure (2.6) corresponds to the depletion region charges due to the exposed, fixed immobile dopants. The depletion width typically extends over several hundred nm. At some point the band bending is twice the Fermi potential $Ø_F$, which is enough for the onset of strong inversion. So the exponential term is multiplied by the minority carrier concentration and become equal to the majority carrier concentration [9]. Hence for band bending beyond this point, it becomes the dominant term, as in the case of accumulation the mobile inversion charge is now increases very strongly with bias, as indicated in equation (2.2), and shown in the figure(2.6).

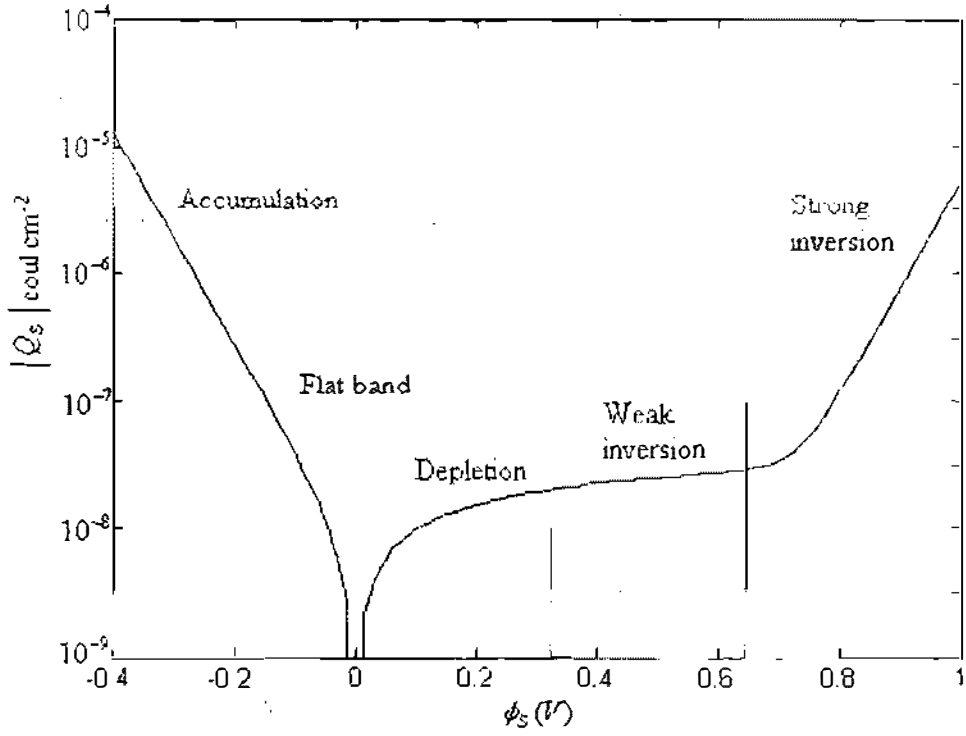

Fig.2.6: Space charge density in the p-type semiconductor as a function of the surface potential, ϕ_S with doping concentration of $1\times10^{17} cm^{-3}$, Flat band voltage 0 V.

Again using the depletion approximation, we can solve for maximum depletion region W as a function of ϕ_S [13].

$$W = \sqrt{\frac{2\varepsilon_S \phi_S}{qN_a}} \qquad 2.12$$

Here W is the depletion width. The depletion region grows with the increased voltage across the capacitor until strong inversion reached. After that, further increases in the voltage result in strong inversion rather than in more depletion. So the maximum value of the depletion width will be [13]

$$W_M = \sqrt{\frac{2\varepsilon_S \phi_{S(inv)}}{qN_A}} \qquad 2.13$$

The charge per unit area in the depletion region Q_d at strong inversion is

$$Q_d = -qN_A W_M \qquad 2.14$$

$$= -2\sqrt{(\varepsilon_S \phi_F q N_A)}$$

The applied voltage must be large enough to create this depletion charge plus the surface potential $\phi_{S(inv)}$. The threshold voltage required for strong inversion is

$$V_T = -(\frac{Q_d}{C_i}) + 2\phi_F + V_{FB} \qquad 2.15$$

Where

$$2\phi_F = 2(\frac{KT}{q}) \ln \frac{N_A}{N_i} \qquad 2.16$$

This assumes that the negative charge at the p-type semiconductor's surface Q_S for the onset of inversion is mostly due to the depletion charge Q_S. the threshold voltage represents the minimum voltage required to achieve strong inversion, which is an extremely important quantity for MOS transistor.

2.3 Potential balance in a MOS Structure

Let us assume that we have a p-type substrate. Here any value of gate voltage (V_{GB}) will have an impact on the semiconductor. Basically there are four kinds of drop across the MOS structure.

1. The voltage of external voltage source, V_G
2. The potential drop across the oxide, V_i
3. Surface potential, ϕ_S
4. Work function difference, ϕ_{MS}

Applying KVL in the MOS structure

$$V_G = V_i + \phi_S + \phi_{MS} \qquad 2.17$$

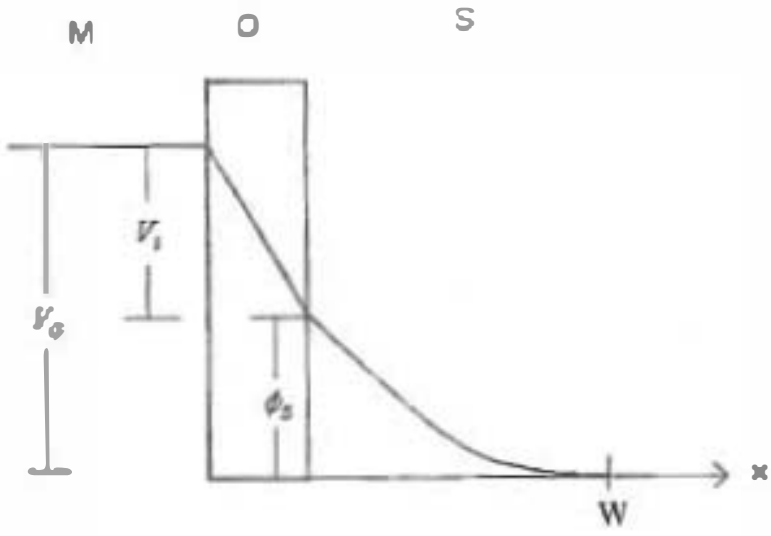

Fig 2.7: Approximate distribution of electrostatic potential in MOS structure for zero ϕ_{MS}.

As ϕ_{MS} is a known amount, any change in V_G will balanced by V_i & ϕ_s [12, 13].

The voltage across the insulator is related to the charge on either side, divided by the capacitance [13]

$$V_i = \frac{Q_s d}{\varepsilon_i} \qquad 2.18$$

$$= \frac{Q_s}{C_i}$$

Here ε_i and 'd' are the permittivity and width of the insulator respectively. C_i is the insulator capacitance per unit area. The charge Q_s will be negative for n channel for positive V_i.

2.4 Capacitance of ideal MOS Capacitor

The capacitance-voltage characteristics is voltage dependent (Fig 2.8), we must use the more general expression [13]. Semiconductor capacitance C_S is given by

$$C_S = \frac{dQ_S}{d\phi_S} \qquad 2.19$$

Now the semiconductor capacitance itself can be determined from the slope of the Q_S versus ϕ_S plot (Fig. 2.6). For negative voltage, holes are accumulated at the surface. The structure appears almost like a parallel plate capacitor, dominated by the insulator properties $C_i = \varepsilon_i / d$. As the voltage become less negative, the semiconductor surface is depleted. Thus a depletion layer capacitance C_d is added in series with C_i.

$$C_d = \frac{\varepsilon_s}{W} \qquad 2.20$$

Here ε_S is the semiconductor permittivity and 'W' is the width of the depletion layer. So the total capacitance is

$$C_G = \frac{C_i C_d}{C_i + C_d} \qquad 2.21$$

The capacitance decreases as W grows until finally inversion is reached at V_T in depletion region, the small signal semiconductor capacitance is given by equation (2.19) which gives the variation of the (depletion) space charge with surface potential. Since the charge increases as ~ $\sqrt{\emptyset_s}$, the depletion capacitance will obviously decrease as $1/\sqrt{\emptyset_s}$ [13].

If we continue to increase the positive gate voltage the downward band bending would further increase. In fact, a sufficiently large voltage can cause so much band bending that it may cause the midgap energy E_i to cross over the constant Fermi level E_F. When this happens the surface behaves like n-type material with an electron concentration given by Eq. (2.2). Note that this n-type surface is formed not by doping but instead by inversion of the original p-type substrate due to the applied gate voltage. This is referred to as the inversion condition. The surface is inverted as soon as $E_F > E_i$. This is called the weak inversion regime because the electron concentration remains small until E_F is considerably above E_i. If we further increase V_G the concentration of electrons at the surface will equal, and then exceed, the concentration of the holes in the substrate. This is called the strong inversion regime.

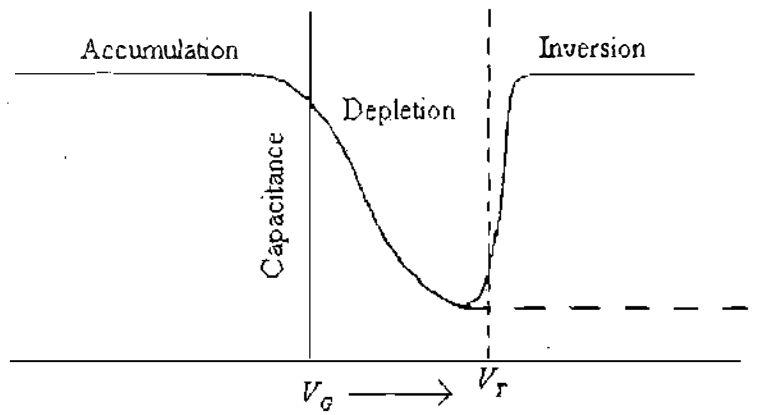

Fig 2.8: Capacitance-voltage relation for a MOS capacitor. The dashed curve for V_G > V_T is observed at high frequencies. And the solid curve is for low frequencies.

Chapter 3

Proposed Numerical Model for MOSFETs with Non-Uniform Substrate Doping

3.1 Model derivation

In order to model 1D MOS capacitor with non-uniform doping we need to solve Poisson's equation numerically. The Poisson's equation is given by [12]

$$\frac{d^2\phi}{dx^2} = -\frac{q}{\varepsilon_s}(p(x) - n(x) - \delta \times N_{SUB}(x)) \qquad 3.1$$

$p(x)$ and $n(x)$ respectively are the hole and electron concentrations and $\delta \times N_{SUB}(x)$ is the concentration for ionized impurities, with $\delta = 1$ for p-type and $\delta = -1$ for n-type semiconductor . The equation above gives a potential $\phi(x)$ for the given charge density in the substrate with the boundary condition; $\phi(0) = \phi_S$ at the oxide/semiconductor interface and $\phi(\infty) = 0$ in the deep substrate or bulk. As we are using p-type substrate so $\delta = 1$.

As with respect to our any arbitrary non-uniform doping concentration intrinsic concentration is negligible, the simplified formula will be for depletion region

$$\frac{d^2\phi}{dx^2} = \frac{q}{\varepsilon_s}(N_{SUB}(x)) \qquad 3.2$$

Now integrating equation 3.2 we have the electric field profile,

$$\frac{d\phi(x)}{dx} = \frac{q}{\varepsilon_S}\int(N_{SUB}(x))dx \qquad 3.3$$

It should be kept in mind that

$$F(x) = -\frac{d\phi(x)}{dx}$$

As we know with any bias voltage there will be a corresponding electric field in the semiconductor-oxide surface. In our numerical model this surface electric field F_S is an input parameter and electric field equation becomes,

$$F(x) = F_S - \frac{d\phi(x)}{dx} \qquad 3.4$$

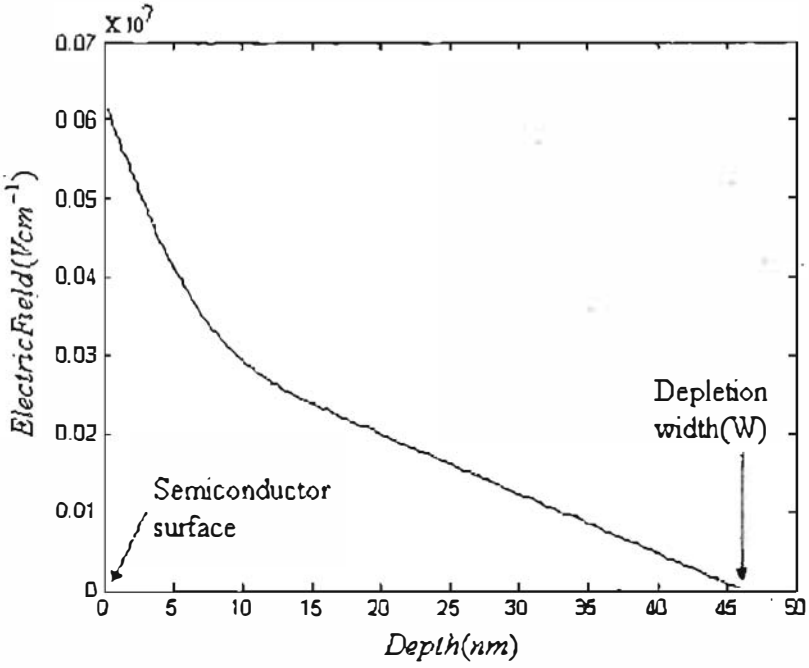

Fig. 3.1 Distribution of electric field in a non-uniform doped MOS capacitor.

In the electric field profile in substrate after a certain distance from surface electric field becomes zero (Fig. 3.1). From here we can determine the depletion width for non-uniform doping profile. This distance (W) is the depletion width for a given surface electric field (F_S). In our model we approximate that maximum surface potential can be equal to $2\phi_F$. We have to choose this surface electric field F_S which makes the surface potential $\phi_S = 2\phi_F$ and it will make depletion width $W = W_M$. After integrating equation 3.4 we get the potential profile

$$\phi(x) = \phi_S - \int F(x)dx \qquad 3.5$$

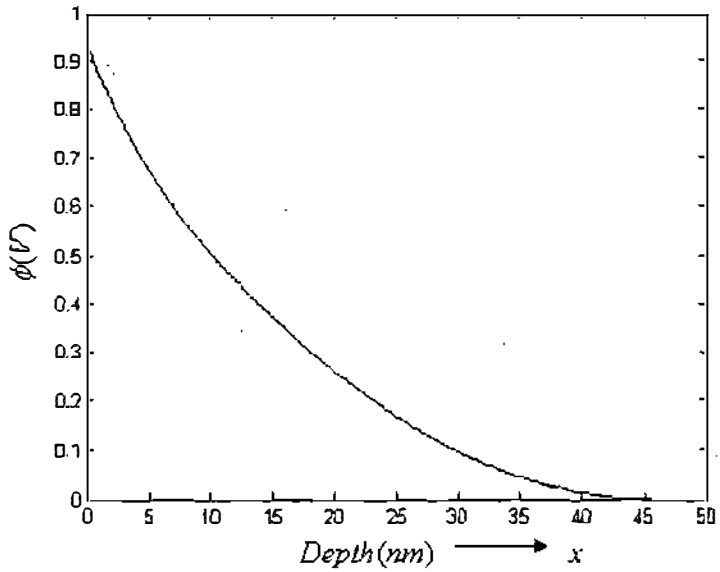

Fig. 3.2 Distribution of potential in a non-uniform doped MOS capacitor.

In Fig. 3.2 at x=0, surface potential $\phi_S = \phi(0) = 2\phi_f$ and at $x = \infty$ $\phi(\infty) = 0$. For the oxide semiconductor interface; the total charge below the oxide is the sum of charge due to the electrons in the inversion layer Q_I and the charge due to the ionized acceptor atoms in the depletion region Q_B [14]

$$Q_C = Q_I + Q_B \qquad 3.6$$

Here Q_C, Q_I and Q_B represent charge per unit area. Depletion charge can be calculated by equation 3.7 [14].

$$Q_B = -q \int_{x=0}^{x=W_M} N_{SUB}dx \qquad 3.7$$

From equation 3.5 $\phi(x)$ is the potential with respect to the bulk. So the electron concentration at any x is given by,

$$n(x) = n_0 e^{q\phi(x)/KT} \qquad 3.8$$

n_0 is equilibrium minority carrier concentration. We now evaluate Q_I. Consider first the electrons in the inversion layer. At any point of ordinate x the electron concentration $n(x)$ will be given by equation 3.8. As one goes away from surface, $\phi(x)$ decreases from ϕ_S towards zero and $n(x)$ decreases rapidly owing to its exponential dependence on $\phi(x)$. Hence, we can assume that below $x = W_M$ the electron concentration will be negligible. Practically all of the free electrons are then contained in a layer between $x = 0$ and $x = W_M$. The inversion charge per unit area Q_I is given by,

$$Q_I = -q \int_{x=0}^{x=W_M} n(x)dx \qquad 3.9$$

Similarly for accumulation bias hole concentration at any x is given by

$$p(x) = p_0 e^{-q\phi(x)/KT} \qquad 3.10$$

If substrate is p-type we can assume $p_0 \approx N_B$. N_B is the back ground doping concentration. The accumulation charge per unit area Q_A is given by,

$$Q_A = q \int_{x=0}^{x=W_M} p(x)dx \qquad 3.11$$

In a MOSFETs potentials are well balanced for a given gate voltage V_{GB}. Expression of V_G is written as

$$V_{GB} = V_{FB} + \phi_S + V_I \qquad 3.12$$

Here V_{FB} is flat band voltage and V_I is voltage across the insulator. As the charges have been calculated as well as the gate voltage, gate capacitance C_G can be calculated by

$$C_G = \frac{dQ_C}{dV_{GB}} \qquad 3.13$$

Chapter 4

Model Simulations

4.1 Results

A n^+ poly-silicon/SiO_2 / p-silicon structure is used for this study. Here oxide thickness has been assumed to be 3 nm. Non-uniform step and Gaussian doping profiles are considered. Current CMOS technologies make use of halo or ion implants to reduce short-channel effects [15] [16] and to control threshold voltage and punchthrough effect [17]. For ion implantation Gaussian doping profile is formed automatically. But step doping profile formation is done intentionally for better performance and control [6]. This result is compared with average uniform doping profile. Poly-silicon depletion effect has been avoided. Flat band voltage, V_{FB} is -.2 V.

4.2 Simulation with step doping profile

Formation of step doping will arise two cases [18]. When the gate bias voltage V_{GB} is such that the depletion depth x_{DM} is less than the depth of the implant x_i (i.e. $x_{DM} < x_i$) the substrate can be considered to be uniformly doped with concentration N_S.

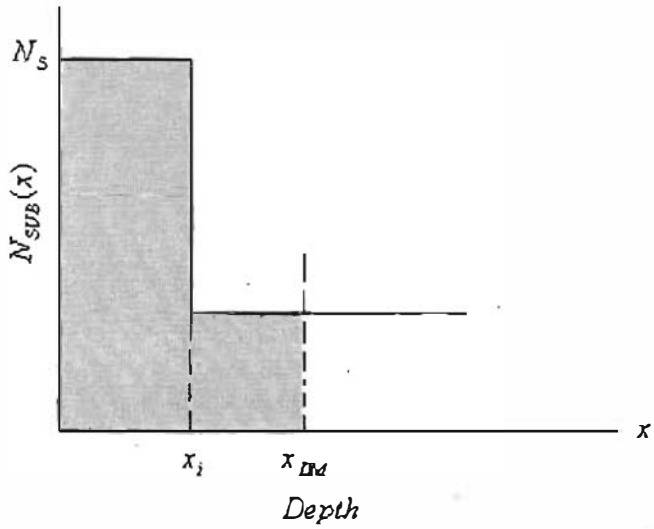

Fig. 4.1 Step doping profile for an n-channel MOSFETs

When V_{GB} is such that x_{DM} lies outside x_j (Fig. 4.1) (i.e. $x_{DM} > x_j$) x_{DM} has now to be determined from the high-low step doping profiles. Analytical equations are no longer works in this case.

Now let us consider the step doping profile in Fig. 4.2. Here this step profile can be formed by one or more low dose shallow implants into a uniformly doped substrate of concentration $1\times10^{17}\ cm^{-3}$ [19]. The implanted profile is approximated by constant doping of $5\times10^{17}\ cm^{-3}$ from surface to 30 nm depth. Step doping profile introduces a new surface electric field gradient on the interface of 30 nm depth (Fig. 4.3).

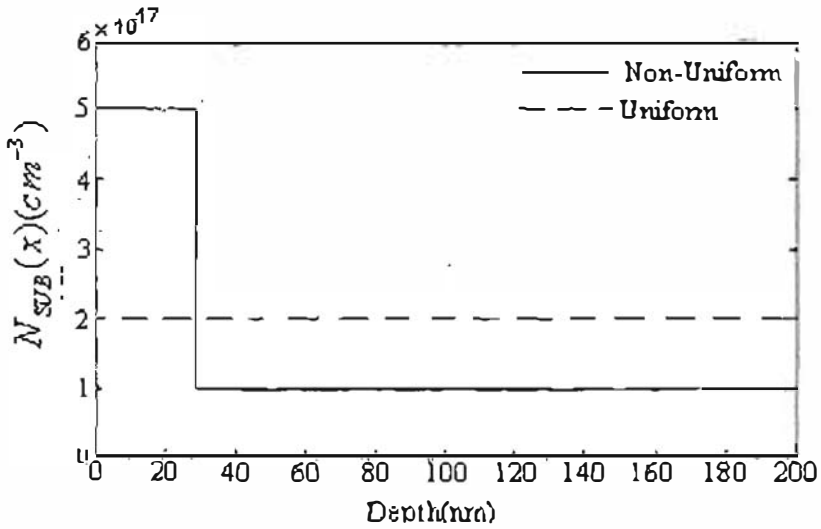

Fig. 4.2: Step non-uniform doping profile (solid line) and uniform doping profile (dashed line) used for simulation.

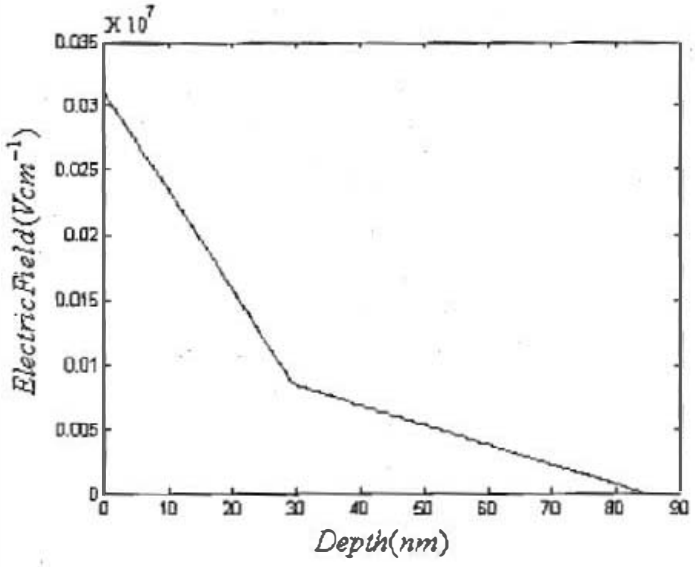

Fig. 4.3 Electric field profile in substrate for step doping profile of figure 4.2.

One thing to note here that from the analytical equation of W_M we find that for uniform doping ($2\times10^{17}\,cm^{-3}$) (Fig. 4.2) we have the maximum depletion is 74 nm. But the above figure (Fig. 4.3) shows us that after 83 nm the electric–field becomes zero. So we have W_M is 83 nm for the step doping profile.

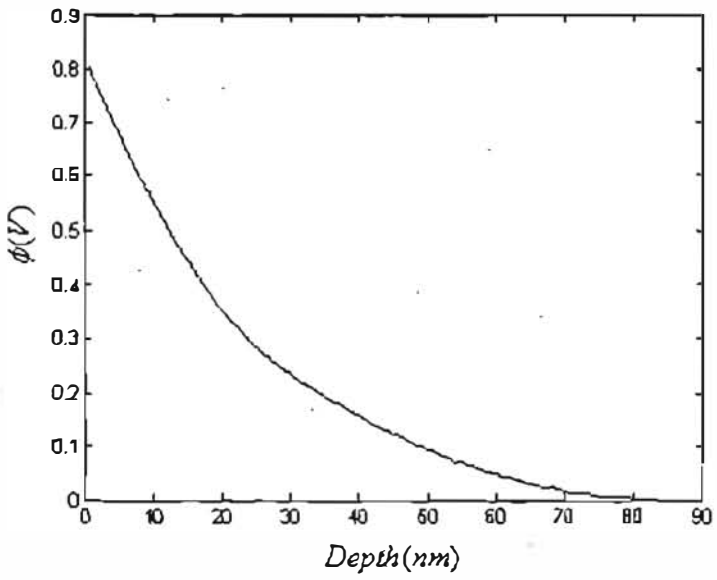

Fig. 4.4 Potential distributions in substrate for step doping profile.

From potential distribution curve in Fig. 4.4 we can see as we go into the depth of the substrate potential decreases and at maximum depletion width W_M potential is zero. After using equation 3.8, 3.10, 3.11, 3.12 we can calculate all charges. By differentiating with respect to gate voltage we can generate C-V curve (Fig. 4.5) for non-uniform step doping profile.

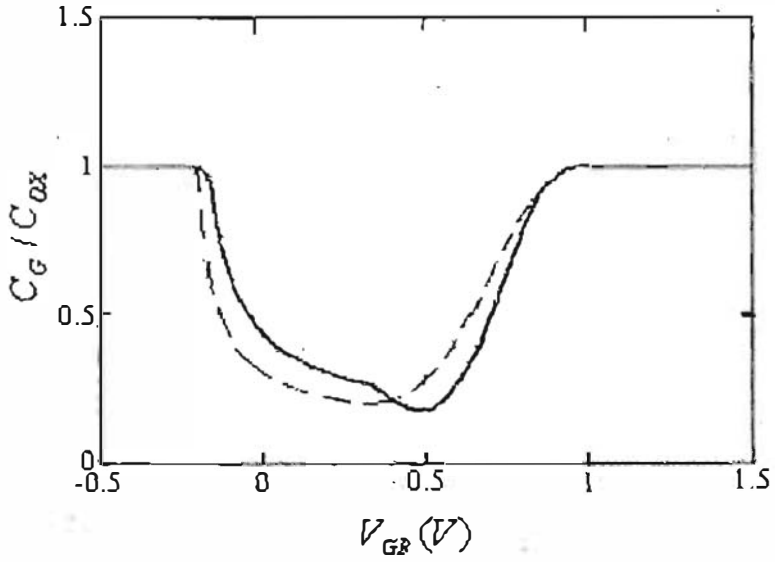

Fig. 4.5 C-V curve for both uniform and non uniform doping profile (Dotted line is the uniform and solid line represents the non-uniform doping profile).

In this figure we can see that the step doping profile has a significant effect in the depletion region, a visible change of capacitance occurs at flat band voltage. Another change seen is in minimum capacitance, which occurs at a higher voltage from non-uniform doping. A bump is seen at about 0.4V which represents the depletion region crossing 30 nm. The curve is shifted to its right which means threshold voltage is increased. Another important point to note that at the edge of accumulation and depletion the curve shows abrupt transition. This is because of we assume maximum surface potential is equal to $2\phi_F$. The curve for constant $\phi_S = 2\phi_F$ represents the classical gate capacitance model where $\phi_S = 0$ in accumulation and $\phi_S = 2\phi_F$ for $V_{GB} > V_T$ [20].

4.3 Simulation with Gaussian doping profile

When ions are implanted into the channel, the implanted profile can be fairly accurately approximated by the following Gaussian distribution function

$$N_{SUB}(x) = N_0 \exp[-\frac{(x-R_p)^2}{2\Delta R_p^2}] + N_B \qquad 4.1$$

Where,

$N_0 = D_i/(\Delta R_p\sqrt{2\pi})$ is the maximum concentration and occurs at $x = R_p$

x= the depth measured from the oxide-silicon interface,

R_p= projected range (average penetration depth),

ΔR_p= straggle (standard deviation)

D_i= dose, i.e., number of implanted ions per unit area.

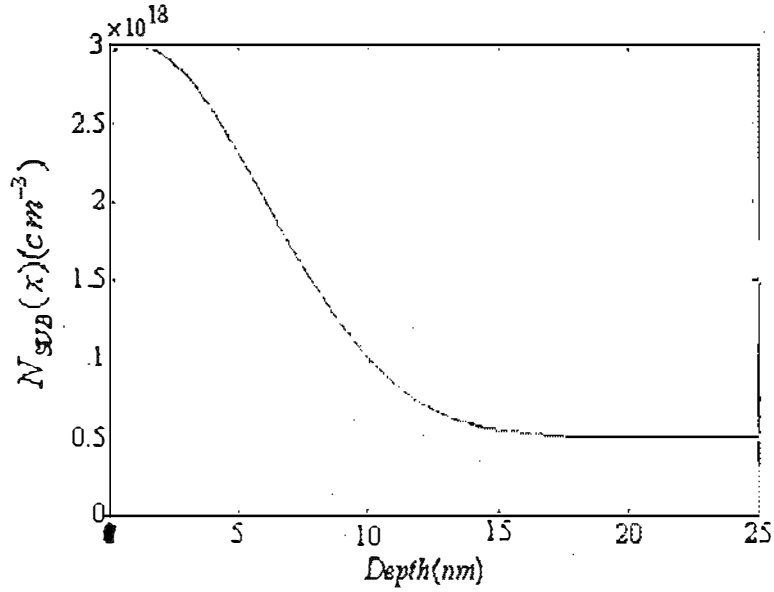

Fig. 4.6 Non-uniform (Gaussian) doping profile used for simulation

We use a Gaussian doping profile with background doping of $5\times10^{17}\,cm^{-3}$(Fig. 4.6). Maximum doping concentration at surface is $3\times10^{18}\,cm^{-3}$. Transition width of this Gaussian doping profile is 17 nm.

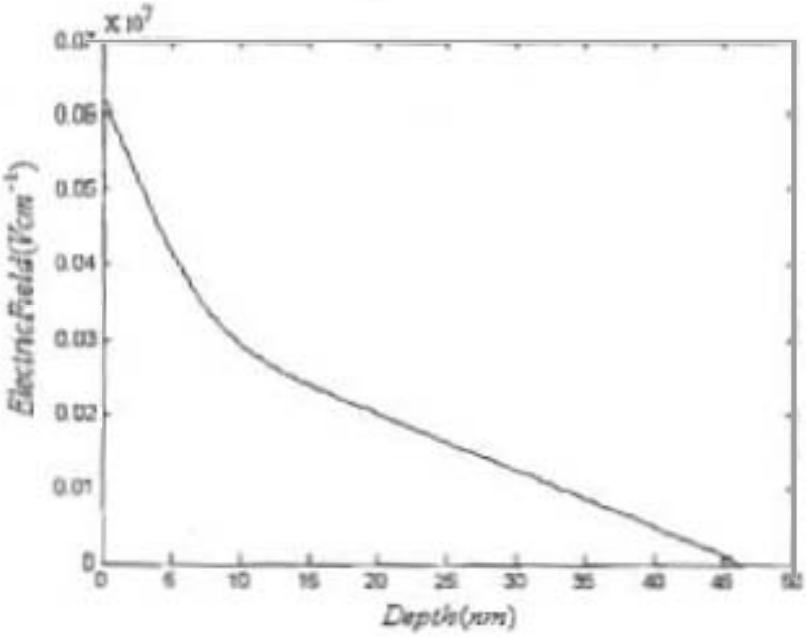

Fig. 4.7 Electric field profile in substrate for Gaussian doping profile for $\phi_s = 2\phi_F$

This Gaussian doping profile of figure 4.6 is another realistic non-uniform doping profile. The solution of Poisson's equation gives us electric field distribution in substrate (figure 4.7). From this figure 4.7 we find W_M is 46 nm. We compared this result with an average uniform doping of $8.425\times10^{17}\,cm^{-3}$. For this average uniform doping W_M is 37.78 nm. For this Gaussian doping profile C-V curve is generated in Fig. 4.9.

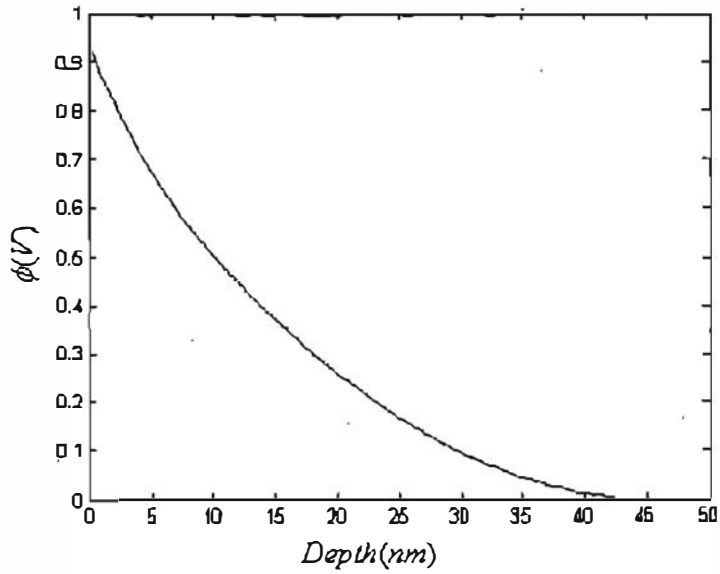

Fig. 4.8 Potential distributions in substrate for Gaussian doping profile

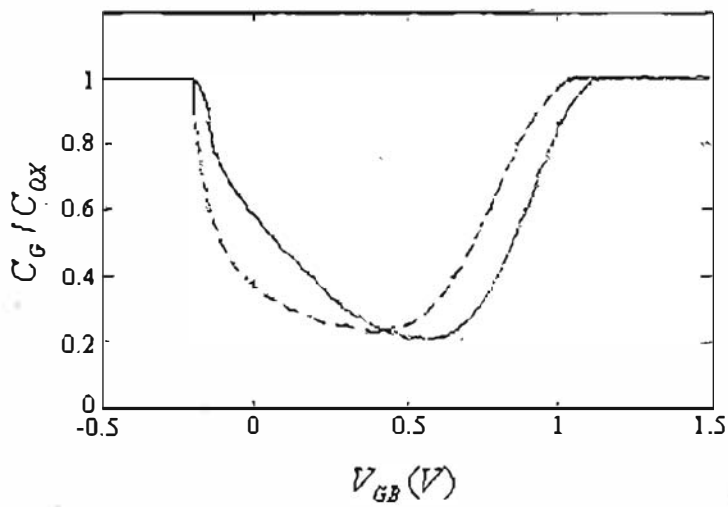

Fig. 4.9 C-V curve for both uniform and non uniform doping profile (Dotted line is the uniform and solid represents the non-uniform doping profile).

For this Gaussian doping profile C-V curve is generated in figure 4.9. We compared this result with an average uniform doping of $8.425 \times 10^{17} cm^{-3}$. For this average uniform doping W_M is 37.78 nm. It also shows a significant influence in the weak accumulation and around the depletion region. Both non-uniform doping profiles caused a shift of the C-V curve to the right. No bump is visible for the C-V characteristics with Gaussian doping profile. But the minimum capacitance is lower for the Gaussian doping profile. Threshold voltage also increases for Gaussian doping profile.

Chapter 5

Conclusions

5.1 Summary of the work

The effect of realistic non-uniform substrate doping profiles on gate C-V characteristic has been studied in this thesis. A semi-classical numerical model is used. Non-uniformity of doping profiles has a significant effect on C-V curve. The effect also depends on the nature of non-uniform doping profile.

5.2 Suggestion for future work

We consider here maximum surface potential ϕ_s can be equal to $2\phi_s$. But in real case ϕ_s should be solved. These will make our C-V curve more realistic. Quantum mechanics has not been introduced in our thesis. It affects C-V characteristics a lot. A good prospect line in this work as it deals with reliable approaches of modeling the ultrathin oxide MOSFETs. Further studies may lead to a set of more accurate expression. In many cases approximately equal have been used and this leaves a scope for the determination of perfect energy band distribution of interface trap charges I ultrathin MOSFETs. There are various modeling issues that await exploration in nanoscale MOSFETs. First, numerical device simulation poses several ongoing challenges. As transistor have reached dimensions approaching the mean distance between collisions, it is strongly desirable to fully exploit a multi-dimensional Poission-Schrödinger solver that trits electrons as waves traveling across the device. Modeling and characterization of high gate field effects-gate direct tunneling (DT), polysilicon depletion and gate induced drain leakage (GIDL) are crucial. These will affect the C-V characteristics from ideal condition.

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