East West University

"A Semi-Analytical Model for III-V Semiconductor Quantum Well Field Effect Transistors"

By

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Md. Shajedur Rahman

In partial fulfillment of the requirements for the degree of

Bachelor of Science in Electrical and Electronic Engineering

Spring 2014

Department of Electrical and Electronic Engineering

Faculty of science and engineering

East West University

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Abstract

Si MOS technology is reaching near the fundamental scaling limit. New materials are being explored to sustain the continual scaling of MOSFETs in the deca-nanometer regime or even lower. III-V semiconductor materials are potentially attractive alternatives to Si.

In this thesis we propose a semi-analytical model for the current-voltage characteristics of III-V semiconductor quantum well field-effect transistors (QWFET). The model calculates the quantized states in the well through numerical solution of one dimensional Schrodinger's equation using the finite difference method. Channel carrier density and drain current as functions of gate and drain voltages are calculated analytically. Results of sample calculations are presented for an InGaAs QWFET. It is expected that the model will be useful in qualitative studies of the device trends.

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Approval

The thesis titled "A Semi –Analytical Model for III-V Semiconductor Quantum Well Field Effect Transistors" submitted by Md. Samiul Islam (2009-2-80-009), and Md. Shajedur Rahman (2009-2-80-034), session Spring 2014, has been accepted satisfactory in partial fulfillment of required degree of Bachelor of Science in Electrical and Electronic Engineering on April, 2014.

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Authorization Page

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Chapter 1. Introduction

As conventional silicon transistors are reaching physical size limit, new materials and device structures are being assessed. Among the different materials proposed to continue the microelectronics revolution, III-V semiconductor technology is attracting attention due to its unique optical and electronic properties. As it has been well known for decades, the electron mobility of III-V compounds is much higher than the corresponding one in silicon [1].

1.1 Background

There has been tremendous progress made recently in the research of novel electronics for future applications [2]. Silicon has been used as the main material in the Integrated Circuits (IC). The device scaling is an important issue in semiconductor IC industries. Recently this continual device downsizing is becoming increasingly difficult because of both fundamental limitations and practical considerations as the transistor dimensions are approaching the deca-nanometer range [1]. As a result to attain this limiting size and high performance, high mobility channel materials like Ge and III-V materials have joined in present time. Recently, studies have been carried out on III-V compound semiconductors as potential channel materials for MOSFETs [3].

1.2 Literature review

III-V semiconductors have been used extensively for making high electron mobility transistors (HEMTs) for analog, digital and mixed-signal high-frequency applications. III-V materials are also being actively investigated in MOSFETs for low power or high performance applications. These developments have been driven by the advantage of higher electron mobility and also the benefits of bandgap engineering with nearly lattice-matched semiconductors. Historically, there have been several challenges for III-V semiconductors to be realized for logic applications. Breakthroughs in recent research have partially solved or relieved some of the challenges. The first III-V MOSFET in history, a GaAs MOSFET, was built by the Radio Corporation of America in 1965 [4]. Soon after that it was realized that finding the low defect, thermodynamically stable insulator is the key to III-V MOSFETs. Unlike the perfect interface between SiO_2 and Si, compound semiconductors do not have an ideal native oxide to form a reliable MOSFET structure.

In parallel with the development of surface channel III-V MOSFETs with atomic-layer-deposition (ALD) of gate oxides, a quantum well structure with $In_xGa_{1-x}As$ or InAs as channel layer has attracted a lot of attention. Such quantum well III-V FETs are similar to the traditional HEMT structure widely used in RF CMOS, but their potential for digital circuits have been studied recently. Different from the surface channel MOSFETs, the channel layer in the quantum well structure is kept between two barriers which eliminate the interface issues due to the good interface quality between the channel and the barriers. The quantum well structure has been successfully fabricated on Si wafers with GaAs and $In_xGa_{1-x}As$ gradual buffer layers [5], and has shown very good *I-V* characteristics and scaling behavior [5-9], which is suitable for future post Si CMOS. But there are two big issues related with the III-V quantum well structure. At first the metal gate is deposited on the upper barrier layer which acts as an insulator layer, but such metal/semiconductor forms Schottky barrier which leads to large gate leakage current under both low and high gate biases. This issue has recently been solved with a high k dielectric layer deposited on top of the barrier, which reduces the gate leakage by a factor larger than1000 [10]. Another issue is more serious, the series resistance in the III-V quantum well transistors is about 2~3 times larger than that in up-to-date Si MOSFETs [11-12]. Unless significant advances were made in reducing the series resistance, the excellent intrinsic device performance will be lost as the device will be dominated by large extrinsic resistance with scaling. Another historical challenge for the implementation of III-V CMOS logic is to look for high mobility III-V p-type MOSFETs. Intel has recently reported high performance 40 nm gate length InSb p-channel transistors using the quantum well structures with compressive strain between the InSb channel and the $Al_{0.4}In_{0.6}Sb$ barrier layers [13]. Compared to Si, such p-channel strained InSb quantum well transistors show about 10 times lower power at the same speed, or about 2 times higher speed at matched power. Strain application in III-V therefore, provides a possible solution for p-type transistors in the future. It was estimated that if III-V were to replace Si CMOS, it would be beyond the 15 nm node.

1.3 Objective

Our aim is to develop a semi-analytical model for III-V semiconductor QWFET devices. For this purpose we have considered a device structure which is shown in figure (1.1). We have assumed $In_{0.53}Ga_{0.47}As$ as channel and $In_{0.52}Al_{0.48}As$ as barrier which are lattice matched to InP. Our model provides current voltage characteristics, transconductance,

and carrier concentration of a device easily. In this process we solve the one dimensional time independent Schrodinger's equation numerically to calculate the quantized states in the well. Then analytically calculate channel carrier concentration, drain current and transconductance of the device under our consideration.

Oxide	Al_2O_3	Oxide Layer	2 nm
Cap	$In_{0.52}Al_{0.48}As$	Undoped	3 nm
Barrier	$In_{0.52}Al_{0.48}As$	Undoped	15 nm
Channel	$In_{0.53}Al_{0.47}As$	Undoped	13 nm
Substrate	InP	Undoped	10 nm

Figure 1.1: Structure of the considered QWFET.

Chapter 2. Quantum Well FETs

2.1 Motivation

The silicon MOSFET has been the most important building block of IC for last few decades. It is used to build both switches for digital logic and amplifiers for analog applications. For the improvement in the performance of ICs, the semiconductor industry has been faithfully following Moore's Law [14]**.** It states that the number of transistors incorporated in a chip will approximately double in every 24 months and it has been the guiding principle for the semiconductor industry for over 30 years. Figure (2.1) shows count of transistors over the years and the representation of Moore's Law.

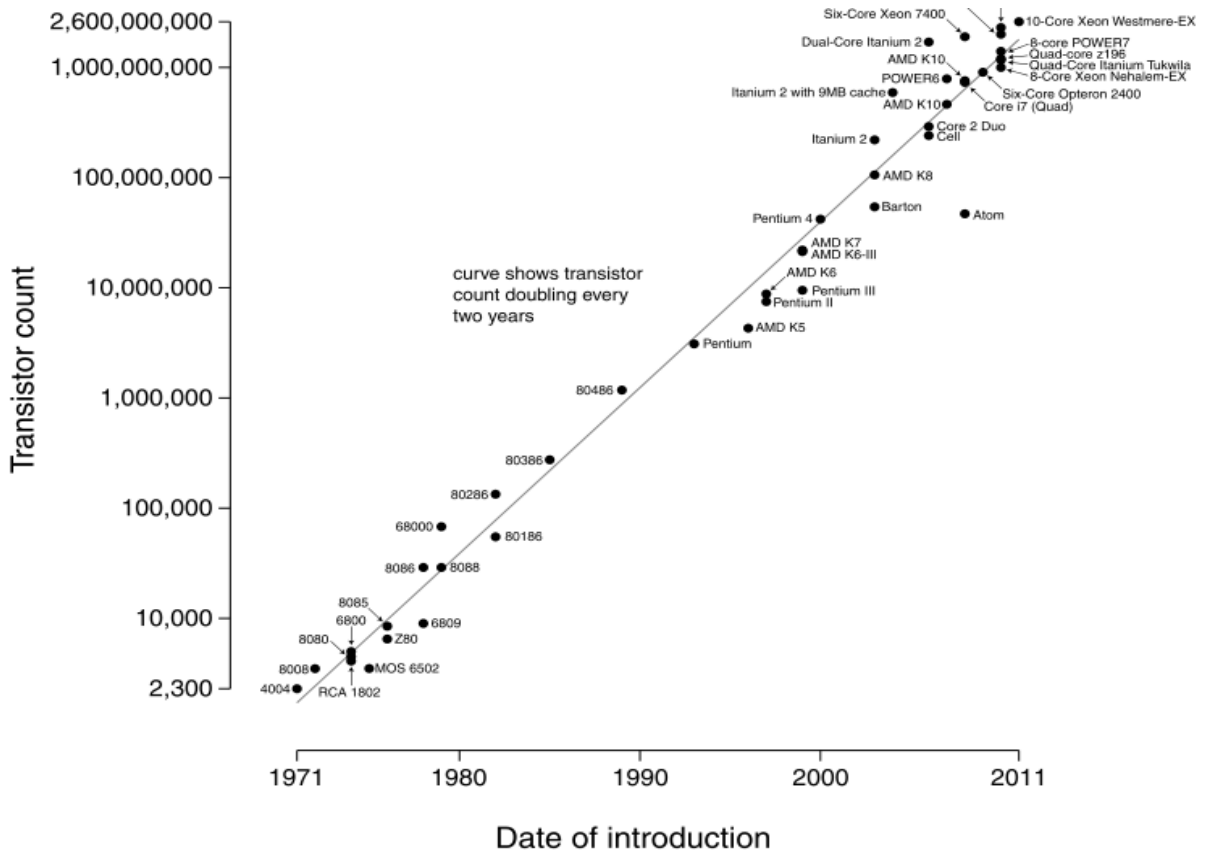

Figure 2.1: Microprocessor transistor count 1971- 2011 and Moore's Law [15].

As a result, the physical dimensions have been continuously shrinking for the last fifty years. This scaling has not only technological benefits but also it reduces cost per transistor through increased device benefits. Figure (2.2) is the demonstration of how the channel length decreased over time following Moore's Law.

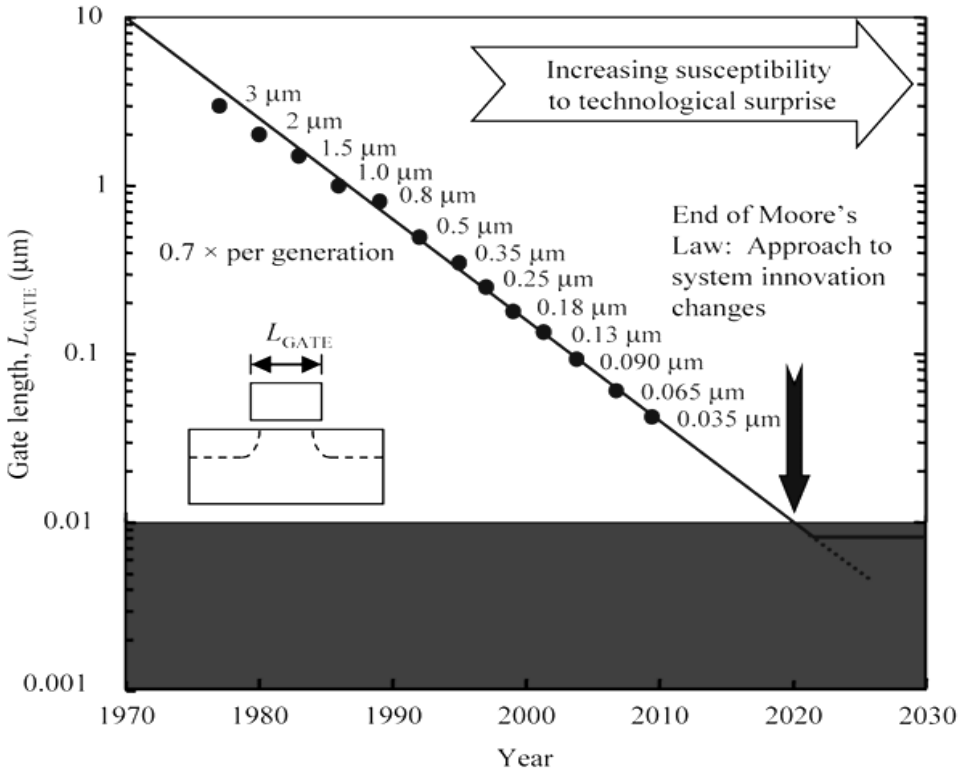

Figure 2.2: Decrease in channel length of MOSFETs over time [16].

III-V semiconductors are highly suitable for optoelectronic applications. Due to their small effective mass and a direct band gap III-V semiconductors have higher electron mobility. This is the main motivation for consideration of III-V materials. Several main challenges however have prevented the implementation of III-V materials for CMOS application for decades. In the early stages silicon was chosen as the channel material of integrated circuits. It was because simply through oxidation (SiO_2) the formation of a stable insulator with a high quality interface was possible. The recent introduction of high-k insulators and metal device contacts in place of polycrystalline Si [17] represent the first change to the fundamental material composition of electronic devices for digital applications. On the other hand, recent research shows that III-V based QWFETs are similar to the high-electron-mobility transistors (HEMTs) already in existence. Due to the relatively matured device technology, and reasonable reliability these have the potential of being the candidate for future n-MOSFETs [18]. It is expected that if III-V semiconductors were to replace Si CMOS, it will be beyond the 15nm node and it should last at least two technology nodes [19].

2.2 Structure

The InP based InGaAs/InAlAs QWFET has been emerging as one of the most promising high speed device. Quantum mechanical effects become important when device geometries are scaled down to nanometer range. Figure (2.3) is the device under our consideration where we have used InGaAs as channel, InAlAs as the barrier and InP as the substrate. Al_2O_3 is used as the oxide layer.

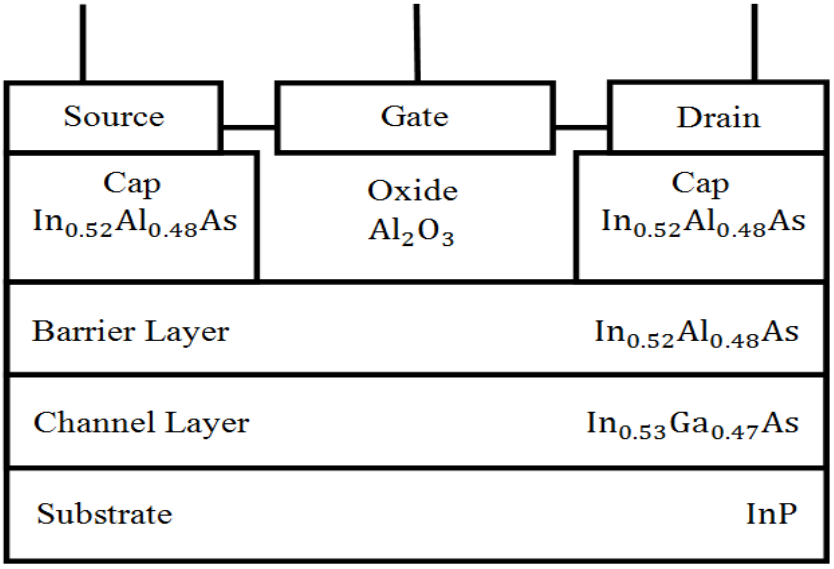

Figure 2.3: The schematic diagram of the QWFET under our consideration.

2.3 Materials

III-V semiconductor materials consist of group III (In, Al, Ga) and group V (P, As, Sb) elements. The III-V compounds have much lower electronic effective masses and therefore higher electron mobility than Si as shown in table (2.1):

Table 2.1: Summary of electron mobility ($\boldsymbol{\mu_e}$), hole mobility ($\boldsymbol{\mu_p}$), and band gap ($\mathbf{E_g}$) of several III-V compound semiconductors [20].

	Si	Strained Si	Ge	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	GaSb	InSb	InP
μ_e (cm^2/Vs)	400	1,000	3,900	8,500	12,000	20,000	3,000	77,000	5,400
μ_P (cm^2/Vs)	160	240	1,800	400	300	500	1,000	850	200
E_g (eV)	1.12	1.12	0.66	1.42	0.74	0.36	0.73	0.17	1.35

2.3.1 InP and InGaAs for III-V FETs:

The tradeoff between mobility and band gap is illustrated through the higher mobility and smaller band gap of InAs and higher band gap but lower mobility of GaAs [21]**.** So $In_{0.53}Ga_{0.47}As$ for its intermediate material properties are often used because it is lattice matched to InP. The basic properties of these two materials are given below in table (2.2) and (2.3) :

Table 2.2: Basic parameters of InP [20].

Crystal structure	Zinc Blende
Dielectric constant (static)	12.5
Effective electron mass m_e	$0.08m_o$
Effective hole masses m_h	$0.6m_o$
Effective hole masses m_{lp}	$0.089m_o$
Electron affinity	4.38 eV
Lattice constant	5.8687 A

Table 2.3: Basic parameters of InGaAs [20].

Crystal structure	Zinc Blende
Dielectric constant (static)	13.9
Energy gap, E_g	0.74 eV
Effective electron mass m_e	$0.041\ m_o$
Effective hole mass m_h	$0.45\ m_o$
Effective hole mass m_{lp}	$0.052\ m_o$
Electron affinity	4.5 eV
Lattice constant	5.8687 A

Chapter 3. QWFET Modeling

3.1 Device Structure

A semi-analytical model is a combination of analytical and numerical models. In a semi-analytical model some variables are analytically calculated by using explicit equations and others are calculated by applying numerical techniques. In modern heterostructure devices the quantized energy levels and wave functions have to be solved to understand the device physics. Analytical solutions of the Schrodinger's equation for the wave functions and energies are only possible for some simple potential structures such as square well, parabolic well etc [22]. But for more complicated structures analytical solution becomes difficult. In such cases, numerical solution is necessary. Figure (1.1) is the device structure under our consideration. We have considered an undoped device with valley degeneracy n_{vi}=1 and equivalent oxide thickness E_{ot}=1 nm. Other variables like carrier concentration, drain current, transconductance etc. are calculated analytically from respective equations.
Figure (3.1) is the conduction band diagram of the device under our consideration.

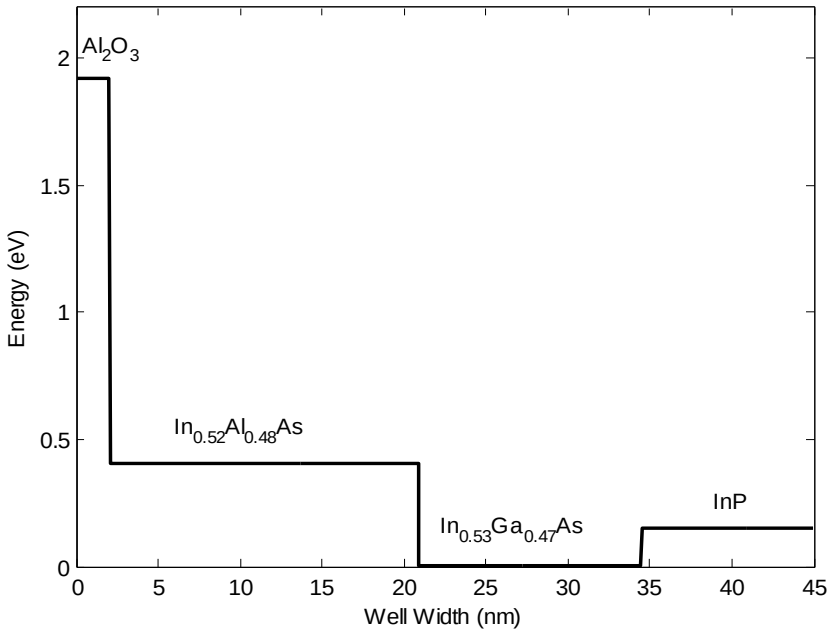

Figure 3.1: Conduction band diagram of the device under our consideration.

3.2 Mathematical Model

To describe a device behavior quantization in well, carrier concentration, drain current are important parameters. Here we have used several equations to solve these parameters.

Analytical models of FETs are important to predict device behavior in circuits, but only a few analytical models have been developed for III-V QWFETs. In our model we have calculated the quantization states in the well trough numerical solution of one dimensional Schrodinger's equation. Channel carrier density and drain current are calculated analytically.

3.2.1 Quantization Effect

Quantization effect is seen in the inversion layer of a MOSFET. To improve the device performance with the continuous downscaling of MOSFET gate length, it requires decreased gate oxide thickness. The quantization effects split electron energy levels into sub bands. The splitting is done in such a way that the lowest of the allowed energy levels for electrons in the inversion layer do not coincide with bottom of the conduction band [23]. We have solved the Schrodinger's equation to find the eigen energy by finite difference method. Details are discussed in Chapter 4.

3.2.2 Carrier Concentration

Let N_i is concentration of charge carriers of sub band *i*, given by equation (3.1) [24].

$$N_i = (n_{vi} m_{di} KT/\pi\hbar^2) F_0[(E_f - E_i)/kT] \tag{3.1}$$

Where $F_0(x) = ln(1 + e^x)$, m_{di} is the density-of-states effective mass in *i*th valley, E_f is the Fermi energy, E_i is the eigen energy of subband.

Considering, The valley degeneracy, $n_{vi} = 1$.The total carrier concentration is the sum of all N_i, $n = \sum N_i$.

3.2.3 Drain Current

Drain Current is computed using equation (3.2) [25].

$$I_d = nev_d \tag{3.2}$$

Where, I_d is the drain current, e is the electron charge, v_d is the drift velocity. Drift velocity $v_d = \mu_d \in$, here $\in$ is the electric field and $\in = V_{dd}/L$, V_{dd} is the drain voltage and L is the channel length.

3.2.4 Transconductance

Transconductance (g_m) is one of the most important factors of a FET. In general, the larger the transconductance for a device, the greater the gain will be. It can be computed by using equation (3.3).

$$g_m = \frac{\partial I_d}{\partial V_g} \tag{3.3}$$

Where, V_g is applied gate voltage.

Chapter 4. Quantum Effect

4.1 Energy Calculation

We have calculated the quantized energies in the channel from the one dimensional time independent Schrödinger's equation (4.1). There are different methods to calculate the eigen values numerically. We have used the finite difference method to calculate the eigen values. We formed the Hamiltonian matrix and by using this we calculated the eigen values. In the sub sections 4.1.1 and 4.1.2 the Schrödinger's equation and finite difference method are discussed.

4.1.1 Schrödinger's Equation

The one dimensional time independent Schrodinger's equation (4.1) can be represented by:

$$-\frac{\hbar^2}{2m}\frac{\partial^2\psi(x)}{\partial x^2} + V(x)\psi(x) = E\psi(x) \tag{4.1}$$

Where, $\hbar$ is the reduced Planck constant, m is the effective mass, ψ is the wave function, $V(x)$ is the potential profile, E is the eigen energy.

Equation (4.1) can also be described as:

$$\hat{H}\psi(x) = E\psi(x) \tag{4.2}$$

Where, $\hat{H}$ is the Hamiltonian operator.

4.1.2 Finite Difference Method

One of the numerical methods of solving the Schrodinger's equation is the finite difference method. The wave function is converted into a column vector. The differential operator is also changed into a matrix form. The simplest way to convert the Schrodinger's equation is to choose a discrete lattice [26].

The wave function ψ(x) can be converted by a column vector $\{\psi_1(x), \psi_2(x) \dots \dots \dots\}^T$

Where T denotes transpose. From here we can write

$\{\psi_1, \psi_2 \dots \dots \dots\} = \{\psi(x_1)\ \psi(x_2) \dots \dots \dots\}$

Where ψ_1 and ψ_2 are different values at x_1 and x_2.

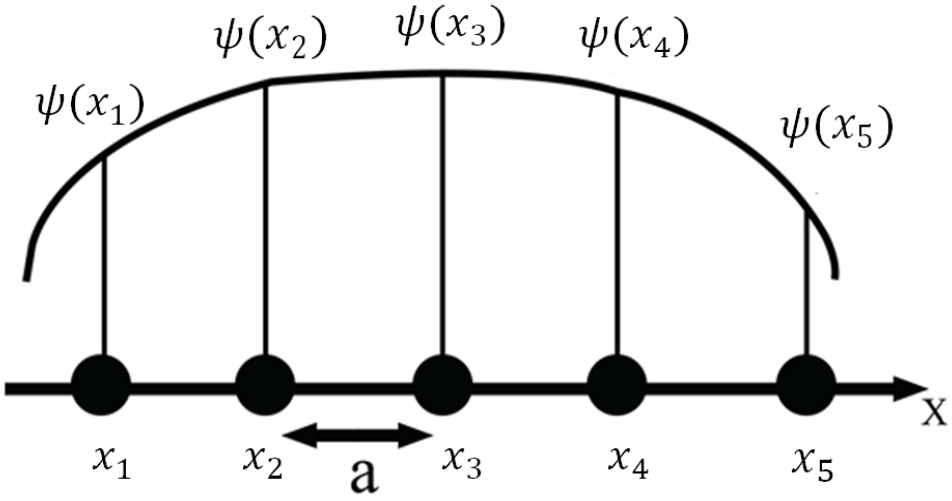

Figure 4.1: A continuous function can be represented by its values at a set of points on a discrete lattice.

Here 'a' is the spacing between two successive points.

Now the matrix representation of Hamiltonian operator will be as in equation (4.3):

$$H_{op} \equiv -\frac{\hbar^2}{2m}\frac{d^2}{dx^2} + V(x) \tag{4.3}$$

In finite difference method the representation of the Hamiltonian operator is shown in equation (4.4):

$$\left(\frac{\partial^2\psi}{\partial x^2}\right)_{x=x_n} \longrightarrow \frac{1}{a^2}[\psi(x_{n+1}) - 2\psi(x_n) + \psi(x_{n-1})]$$

and

$$V(x)\psi(x) \longrightarrow V(x_n)\psi(x_n) \tag{4.4}$$

The Hamiltonian matrix elements are given by the equation (4.5):

$$H_{n,m} = (V_n + 2t_0)\delta_{n,m} - t_0\delta_{n,m+1} - t_0\delta_{n,m-1} \tag{4.5}$$

Where $t_0 \equiv {\hbar^2}/{2ma^2}$ and $V_n \equiv V(x_n)$ and $\delta_{n,m}$ is the Kronecker delta.

So the matrix representation of H will be as equation (4.6).

$$H = \begin{vmatrix} 2t_0 + V_1 & -t_0 & .. \\ -t_0 & 2t_0 + V_2 & -t_0 \\ .. & -t_0 & 2t_0 + V_3 \end{vmatrix} \tag{4.6}$$

4.2 Solution Procedure

Our goal is to find out the characteristics of a III-V semiconductor QWFET using our proposed semi analytical model. We have used III-V materials like InAlAs and InGaAs lattice matched with InP as device materials. Figure (3.1) shows the conduction band diagram of a III-V semiconductor QWFET device under our consideration for calculation using this semi-analytical model.

Al_2O_3 is used as oxide layer. To calculate the thickness of Al_2O_3 equation (4.7) was used.

$$t_{ox} = \frac{E_{ot} \times \in_{r(Al_2O_3)}}{\in_{r(SiO_2)}} \tag{4.7}$$

Where,

t_{ox} is thickness of oxide, $\in_{r(Al_2O_3)}$ is the relative permittivity of Al_2O_3, $\in_{r(SiO_2)}$ is the relative permittivity of SiO_2, Considering effective oxide thickness, $E_{ot} = 1$ nm.

Equation (4.1) is solved to determine the quantized energies of QWFET channel. While calculating quantized energies we have considered the effective mass of InGaAs as $0.045m_0$, where m_0 is the electron rest mass. Work function of InGaAs, InAlAs, InP and Al are 4.5 eV, 4.095 eV, 4.35 eV and 4.25 eV respectively. $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ are assumed to be lattice matched to InP.

Chapter 5. Results and Discussions

5.1 Verification of Results

To verify the accuracy of our calculations, we have compared our results with those of [27] for a simple rectangular well with a 300 meV high barrier, 7.5 nm wide well and $m^* = 0.067m_0$. Figure (5.1) shows the wave functions of the lowest two energies. The lowest two eigen energies are E_1=52.906 meV and E_2=200.595 meV which are very close to the values reported in [27] (E_1=53.474 meV and E_2=199.044 meV) for the same structure. The well structure is given below in figure (5.1).

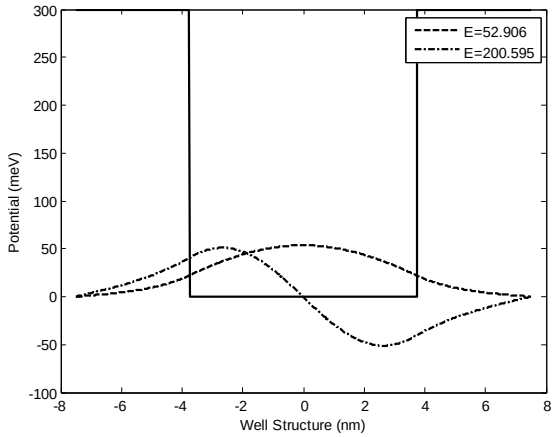

Figure 5.1: Wave functions and the well structure for the comparison with results from [27].

5.2 Eigen Value

Figure (5.2) is the representation of the first eigen energy for figure (3.1) with no applied field, where E_1 is the ground state eigen energy and E_{fs} is the Fermi energy.

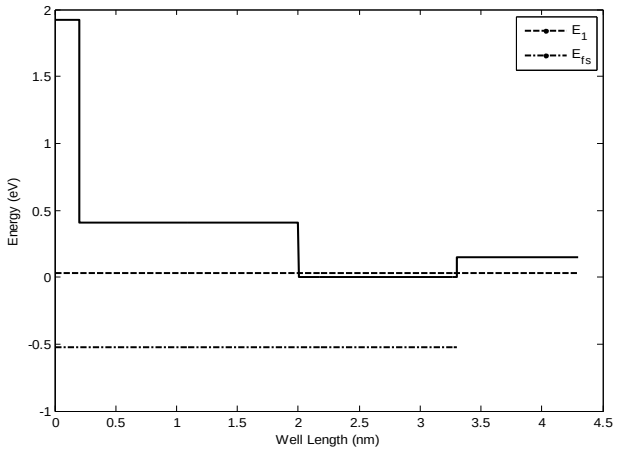

Figure 5.2: Eigen energy and Fermi energy with no applied field.

Again the eigen energy changes with applied field. Figure (5.3) shows the change in eigen energy with a 0.5 V gate voltage applied.

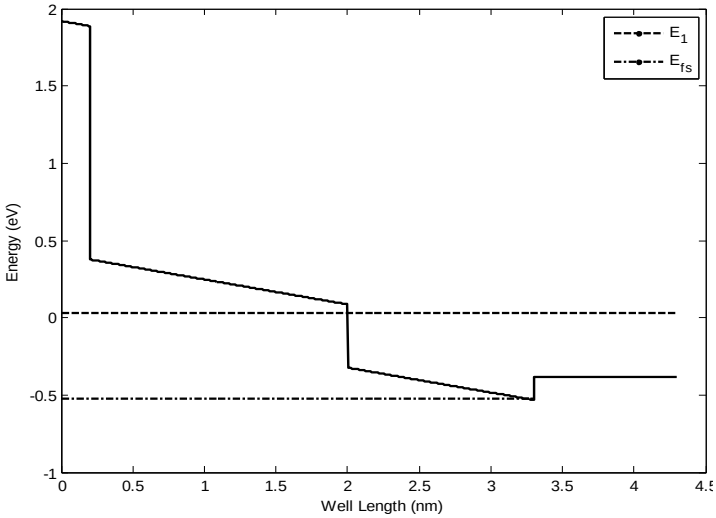

Figure 5.3: Eigen energy and Fermi energy with 0.5 V applied at gate.

We have calculated the eigen energies by varying gate voltage from 0 to 1 V. We also consider fermi level fixed at -0.52eV for simpler calculation though fermi level is not fixed in practical application.

Figure (5.4) shows the change in ground state eigen energy with the change of applied field.

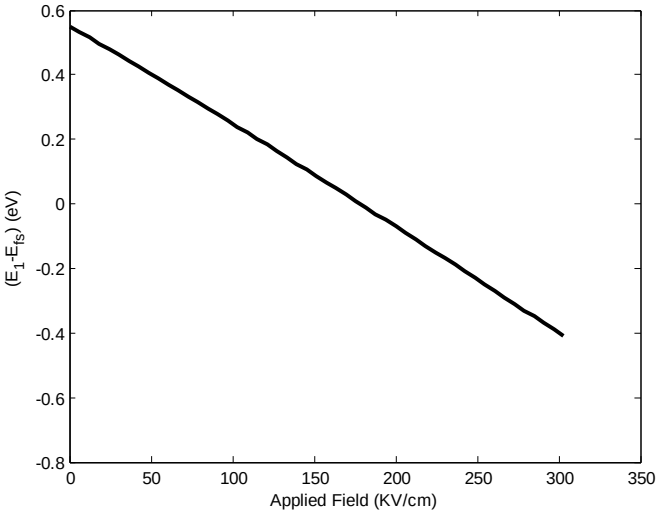

Figure 5.4: Relationship between the difference of ground state energy and Fermi energy with the change in applied field.

5.3 Carrier Concentration

By calculating carrier concentration one can calculate current of a device. Figure (5.5) shows the carrier concentration for different gate voltage which results different eigen energies. This figure also shows total carrier concentration of the device.

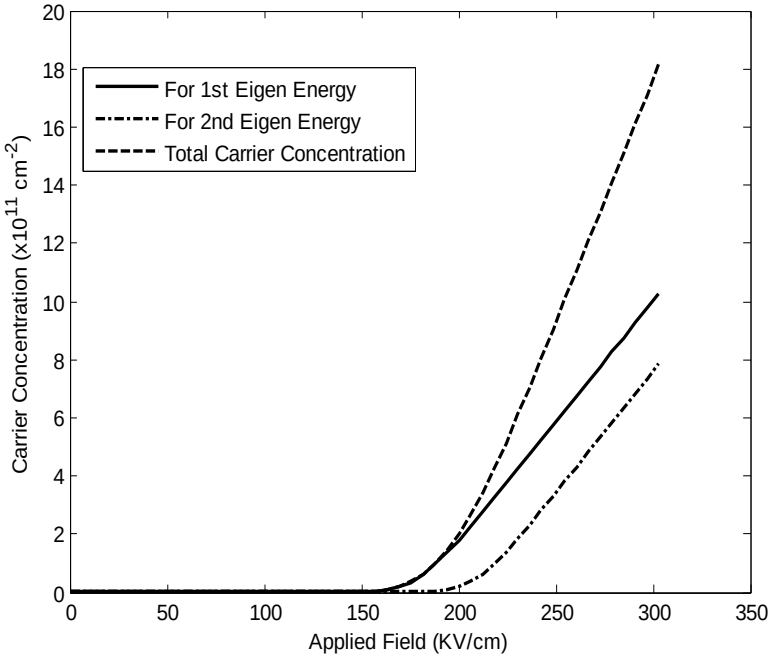

Figure 5.5: Channel carrier concentrations as functions of the electric field along the gate direction.

5.3.1 Current-Voltage Relationship

We have calculated the effect of applied gate voltage (V_g) on drain current (I_d) keeping drain voltage, V_{dd} fixed at 100 mV to find the threshold voltage, V_t. Figure (5.6) shows the current-voltage relationship of the device. This figure is the result of different applied gate voltage.

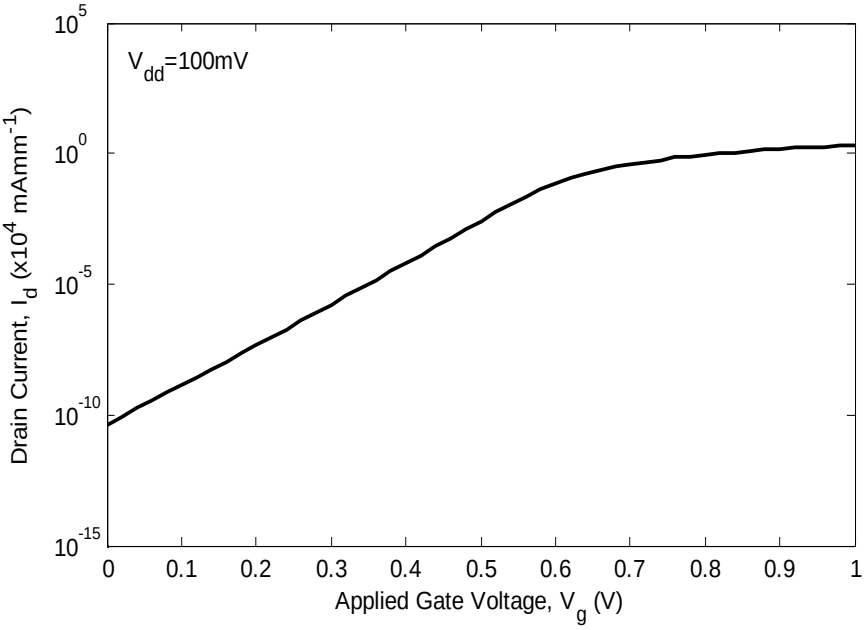

Figure 5.6: Drain current as a function of the gate voltage showing sub-threshold behavior of the device.

And using the current-voltage relation in figure (5.7) we have found threshold voltage, V_t which is 0.63V.

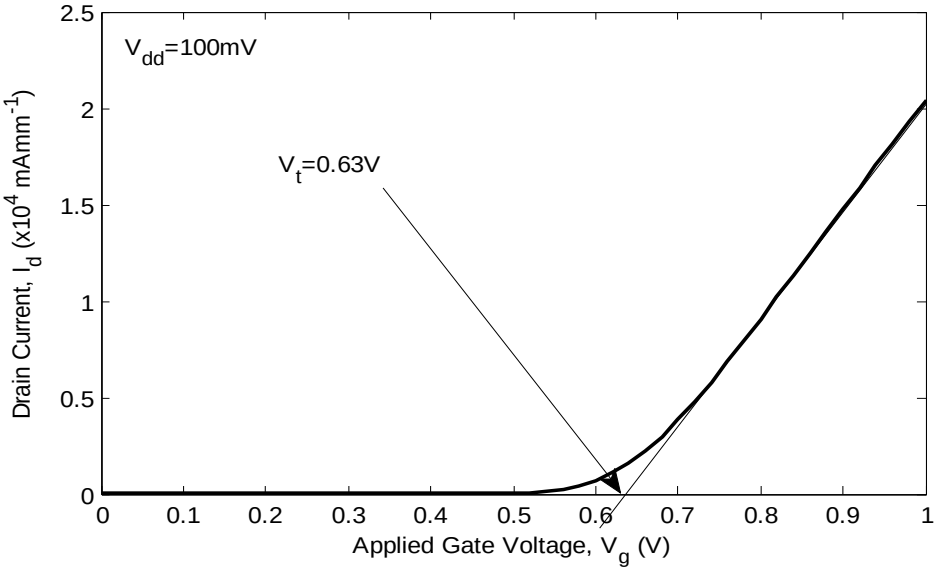

Figure 5.7: Determination of the threshold voltage from the linear relationship between the drain current and the gate voltage where $\boldsymbol{V_{dd}}$ =100 mV.

To calculate the relation between drain voltage (V_{dd}) and drain current (I_d), we assume for simplified calculation that I_d will be saturated when $V_{dd} \geq V_g - V_t$, though in QWFET I_d does not gets saturated at $V_{dd} \geq V_g - V_t$. Figure (5.8) shows the relation between the drain voltage and drain current. Again while doing this calculation we did not consider the effect of drain voltage on the band structure of the device.

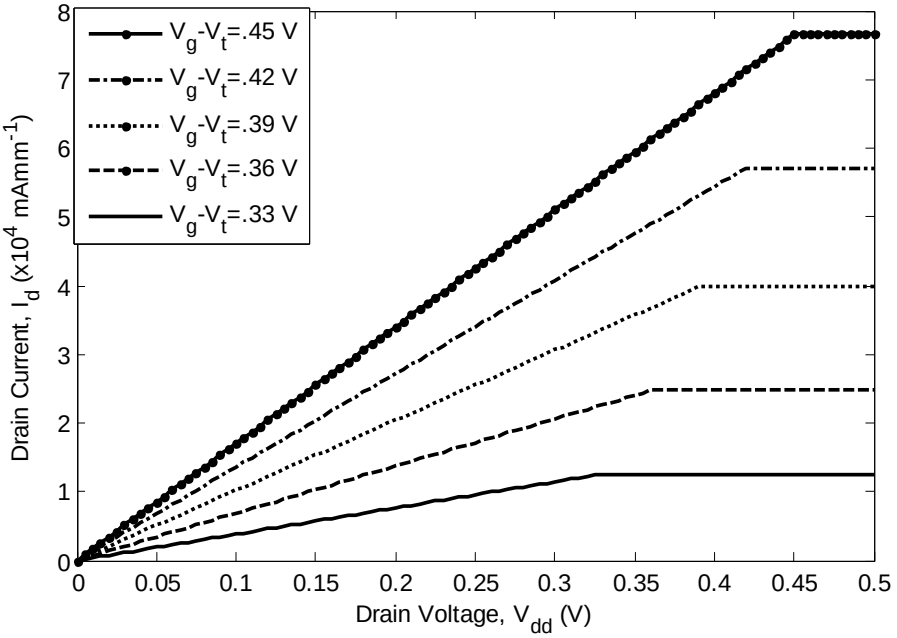

Figure 5.8: $\boldsymbol{I_d - V_{dd}}$ relationship of the QWFET under our consideration.

5.3.2 Transconductance

By using equation (3.5) the following result of the transconductance is obtained. Figure (5.9) shows the transconductance of the device.

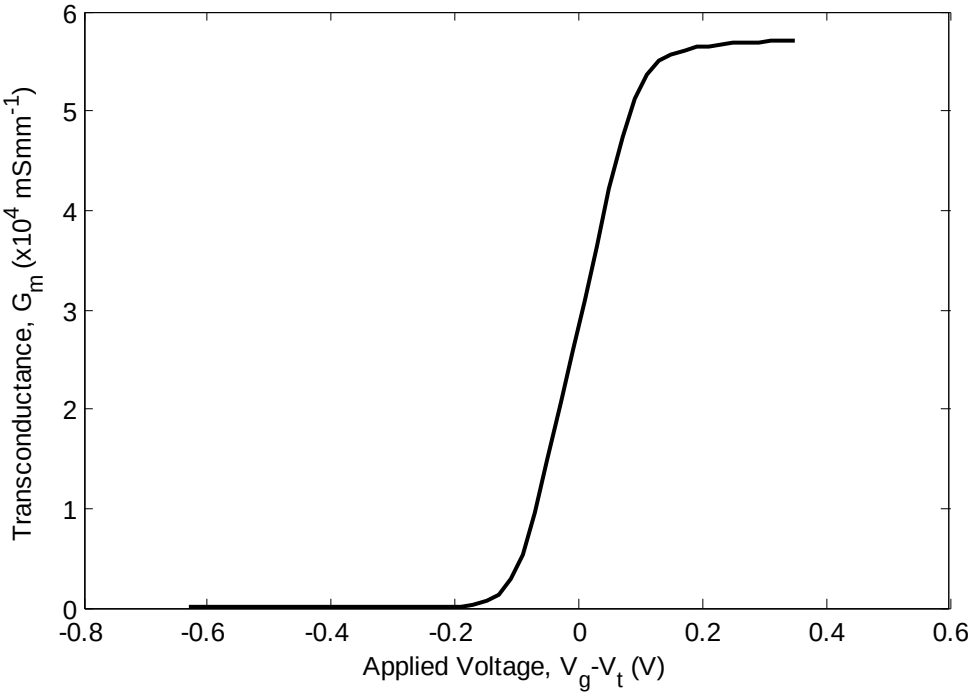

Figure 5.9: Transconductance of the device under our consideration.

Chapter 6. Conclusion

6.1 Summary of Results

III-V semiconductor QWFET is an attractive candidate to replace the Si FET as the scaling limit is approached. We have presented a semi-analytical model for the current-voltage characteristics of III-V semiconductor QWFET. Solutions to one dimensional Schrodinger's equation for quantized states in the channel are obtained numerically using the finite difference technique. The rest of the model is analytical. We have shown sample calculations of carrier concentration and current-voltage relationship of a typical device. This model is useful for qualitatively studying the device performance trends.

6.2 Future Work

The proposed model calculates the quantized states in the well through numerical solution of one dimensional time independent Schrodinger's equation using the finite difference method, where the effect of carriers in channel on the potential is ignored. So to get a complete solution of Schrodinger equation it is very important to consider the effect of carriers on the potential in channel. Carrier mobility is a very important issue for device characteristics which is considered to be a constant in our present model. In fact mobility depends on many things including the gate and the drain voltages. The implementation of this concept is necessary to observe device characteristics more accurately. Again hot carriers are produced as a result of very high fields in the drain region of FETs, and they may compromise operation of the device by generating charged defects in the oxide layer, and by degrading the oxide-semiconductor interface, which is called "hot carrier effect". This phenomenon is also very important to judge device current-voltage relation. In present model variation of the potential profile along source to drain direction is not considered. But to get more accurate result, it is necessary to include the effect of variation of potential profile along source to drain direction in the calculation of the model which can be done by doing a two dimensional analysis. Including above mentioned improvements in the present semi-analytical model, it is expected that the improved model could be a useful tool in quantitative studies of the device trends.

Appendix

We have used following values for different constants.

Table 6.1: Values for different constants.

Serial No	Symbol	Symbol name	Value
1.	m_e	Electron mass	9.1095×10^{-31} kg
2.	$\hbar$	Reduced Plank's Constant	1.0546×10^{-34} Js
3.	κ	Boltzmann Constant	1.38×10^{-23} JK^{-1}
4.	m^*_{InGaAs}	Effective mass of InGaAs	$0.045m_0$
5.	φ_{InP}	Work Function of InP	4.35 eV
6.	φ_{InAlAs}	Work Function of InAlAs	4.095 eV
7.	φ_{InGaAs}	Work Function of InGaAs	4.5 eV
8.	φ_{Al}	Work Function of Al	4.25 eV
9.	m_{di}	The density-of-state effective mass per valley of InGaAs	$0.006m_0$
10.	χ	Electron Affinity of Al_2O_3	2.5 eV

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