The Effect of Dopant and Thickness on the Electrical Behavior of silicon nanowires

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S. M. Fairus Hassan

Spring Semester
April'2013

Abstract

Recently accumulation mode silicon nanowire transistors are in interest due to their near ideal subthreshold slope, large on state current and excellent DIBL. These transistors can be realized even without any dedicated source/drain junctions eliminating the need for costly ultrafast annealing techniques for abrupt junction fabrication and permits one to fabricate device with shorter channel lengths. Silicon nanowire transistors also have significant influence on disease diagnosis as silicon nanowire transistors have been shown to function as high sensitivity transducers due to their smaller size and large surface to volume ratio. However, the accumulation mode transistor behavior of silicon nanowires may depend on doping which in turn may depend on nanowire thickness and hence, effective surface to volume ratio for onset of transistor action may vary with doping. In this work accumulation mode transistor behavior of p-type silicon nanowires are investigated at different doping concentrations and nanowire thicknesses to find out the relationship between NW thicknesses and doping for transistor action. The investigation is done for nanowire thicknesses ranging from 5nm to 100 nm with doping density diverging from $10^{14}cm^{-3}$ to 10^{20} cm^{-3}. It is found that thick nanowire's transistor action is limited only at low doping concentrations whereas thin nanowires are able to exhibit transistor action at high doping densities even at 10^{19} cm^{-3} which is close to source/drain doping of conventional MOSFET. This phenomenon is explained by the gradually decreasing gate modulated volume in the NW with increasing doping concentrations thereby limiting the thickness of nanowires at high doping densities to ensure the whole constricted volume to be affected by gate voltage for onset of transistor action. This research would give insight into the required doping for any particular NW thickness for bio-sensing application and junction less NW transistor fabrication.

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Authorization page

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CHAPTER 1: INTRODUCTION

1.1 Motivation& Objective

Over the past three decades, the exponential growth of the microelectronics industry has been enabled primarily by the continuous scaling [1-3] of metal-oxide semiconductor field-effect transistors (MOSFETs) and device dimensions have been reduced from 10 µm in the 1970's to a present day size of 22 nm [4]. The scaling of transistors is usually plagued with many challenges, such as short channel effects like drain-induced-barrier lowering (DIBL) and degraded sub threshold slope, quantum mechanical gate tunneling, mobility degradation and reliability problems due to random placement of dopant atoms in a host silicon lattice [5,6]. Eventually MOS transistor has been evolved from a bulk MOSFET to fully depleted architectures, planar double gate SOI [7], FINFETs [8] and vertical MOSFETs [9]. Although these architectures have eliminated most of the above challenges, the potential scalability of MOSFETs has still been limited due to fabrication difficulties. Ultra-sharp high doping concentration gradients are required in junctions of these MOSFETs for further scaling down. Due to thermal diffusion and the statistical nature of the distribution of the doping atoms, such junctions represent an increasingly difficult fabrication challenge for the semiconductor industry. Recently transition of silicon nanowires from depletion into accumulation has been shown to exhibit Metal Oxide Semiconductor Transistor (MOSFET) like behavior with excellent functionality [10] which also showed an exciting opportunity for fabricating extremely scaled MOSFETs [10]. In this type of transistors, simple nanowires without any junctions are shown to exhibit transistor behavior due to gate voltage associated depletion to accumulation transition. As such, accumulation mode nanowire transistors eliminate the need for costly ultrafast annealing techniques for abrupt junction fabrication and permit one to fabrication device with shorter channels [10].

Semiconducting silicon nanowire field effect transistors (SiNW-FETs) also have significant influence on disease diagnosis as Si NW–FETs have been shown to function as transducers for label-free high sensitivity and direct electrical detection of Biomolecules [11-23]. This ultra high sensitivity detection can be attributed to their smaller size and large surface to volume ratio, enabling local charge transfers to result in a current change due to a field effect, such as when analytical molecules bind to a specific recognition molecule at the surface of the nanowire [24]. This effect is sufficiently strong that single charge at the surface of the nanowires can be sensed because the depletion or accumulation of charge carriers affects the way entire cross sectional conductor path of these nanostructures [25].

Experimental accumulation mode nanowire transistor so far reported, utilized 20 nm NW thickness with a body doping $10^{19}cm^{-3}$ [10]. While these parameters have shown quite an excellent transistor behavior, the transistor behavior is expected to depend on doping which in turn may depend on nanowire thickness and hence, effective surface to volume ratio for onset of transistor action may vary with doping. This phenomenon is well supported from the vast literature of Si-NW biosensors which show that quite a broad range of NW thicknesses and doping have been used during Si-NW biosensor fabrication [18-22, 26-28]. For a good bio-sensing application, transistor behavior of nanowires is imperative as large change in NW conductance upon application of gate voltage is needed. However, the effect of NW doping and thickness on the transistor behavior of Si-NWs is not yet investigated which is quite essential for a viable biosensor fabrication and also very important for accumulation mode junction less NW transistor fabrication if switching is targeted.

In this work accumulation mode transistor behavior of p-type silicon nanowires are investigated at different doping concentrations and NW thicknesses to find out the relationship between NW thicknesses and doping for onset of transistor action. This research would give insight into the required doping for any particular NW thickness for bio-sensing application and junction less NW transistor fabrication.

1.2 Organization

Chapter 2 provides the necessary background work on accumulation mode silicon nanowire transistors and its application as bio-sensor. A number of research papers on Si-NW biosensor have also been surveyed to gain an understanding on the importance of this work.

Chapter 3 describes device structures, simulation methodology and the required models for the simulation.

Chapter 4 describes the simulated results of the accumulation mode silicon nanowire transistors for nanowire thicknesses from 100 nm to 5 nm and for doping densities diverging from $10^{14}cm^{-3}$ to 10^{20} cm^{-3}.

Chapter 5 focused on the physical explanation for the transition in the device behavior observed for accumulation Si NW transistors at different NW thicknesses and doping.

Finally, in chapter 6, the contribution of this work is summarized and possible areas of future investigations are discussed.

CHAPTER 2: BACKGROUND

This chapter summarizes the background work of accumulation mode silicon nanowire transistors, its application as biosensor and relevant theory associated with this work. Being a novel concept, this type of device attracted attention by several researchers and works have been reported trying to explain the behavior of accumulation mode silicon nanowire transistors. While these works provided some focus on the transistor like behavior of simple nanowires an extensive application could be found on biosensors which have exploited this behavior. These are discussed below:

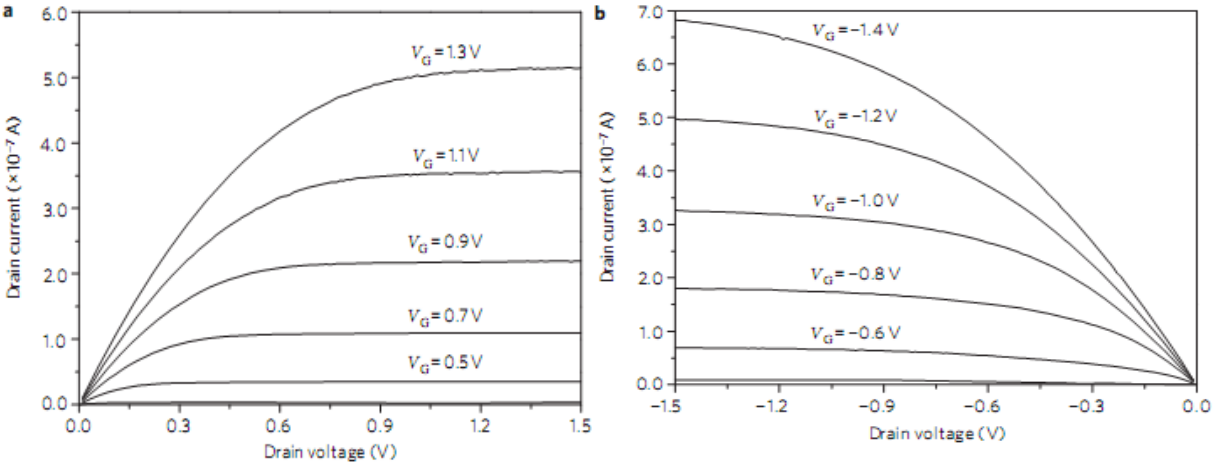


Figure 2.1: Measured output characteristics of junctionless accumulation mode silicon nanowire transistors; a) Drain current versus drain voltage for different values of gate voltages for an n-type silicon nanowire and b) drain current versus drain voltage for different values of gate voltages for an p-type silicon nanowire. The width of the nanowires, W, is 20 nm and the gate length, L, is 1 μm, such that W/L = 0.02 (courtesy: Jean-Pierre Colinge et al. [10])

2.1 Accumulation mode silicon nanowire transistor

Jean-Pierre Colinge et al.[10] first time reported that Si-NWs with a few tens of nanometers wide, thickness of 20 nm and uniform doping concentrations around 10^{19} cm^{-3}, behave as transistor rather than simple conductor. Both p-type and n-type silicon nanowires were fabricated and measured characteristics showed that both n-type and p-type devices exhibited transistor action. These devices showed near ideal sub-threshold slope of 64mv dec^{-1} and quite decent output characteristics. Figure 2.1 and 2.2 show the measured sub-threshold and output characteristics of such accumulation mode silicon nanowire transistors.

To explain the behavior of these devices, a simulation was done [10]. Fig. 2.3 shows the operation principle of n-type accumulation mode silicon nanowire transistor. In the sub-threshold region [Fig.2.3(a)], a highly doped channel is fully depleted. At threshold voltage [Fig.2(b)], current starts to flow through the center of the channel. Above threshold [Fig.2(c)], the channel neutral n-type silicon expands in width and thickness. Further increasing the gate voltage, a completely neutral channel is created [Fig.2(d)] when the gate voltage forces saturation of the drain current.

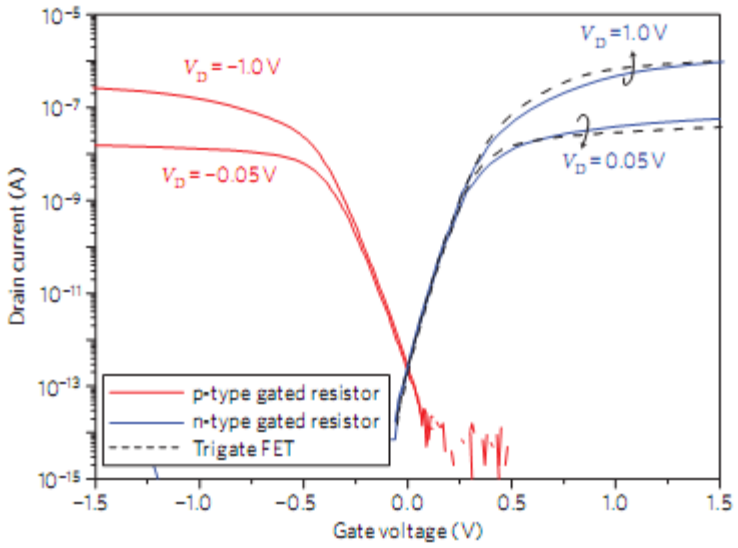


Figure 2.2: Measured sub-threshold characteristics of junctionless accumulation mode silicon nanowire transistors. Drain current versus gate voltage for drain voltages of ±50mV and ±1V for n-type and p-type silicon nanowires. The width of the nanowires are 30 nm and the gate length, L, is 1 µm (courtesy: Jean-Pierre Colinge et al. [10])

A theoretical study on the accumulation mode silicon nanowire transistor was done by Elena Gnani et al. [29] to explain near ideal subthreshold slope, large on state current and excellent DIBL. It is reported that the good subthreshold slope is due to the fixed voltage drop ($\Delta\varphi$) across the silicon nanowire and the oxide under complete depletion of the channel, while lets the potential on the symmetry axis of the nanowire to linearly change with the gate voltage, with a linearity factor equal to 1. The reason for large on-state current which is quite comparable with that of the undoped NW FET with same geometry is attributed to the absence of impurities at the conducting region and reduced surface-roughness scattering. The good DIBL is due to the reason that on-state current injection is modulated by the radius of the neutral region rather than the thermionic injection above the barrier and the electrostatic effect of the drain voltage is screened by the mobile charges within the channel.

In order to understand the behavior of the long-channel accumulation mode silicon nanowire transistor, Juan P. Duarte et. al. [30] proposed that a simple analytical expressions to model the bulk current characteristics of silicon nanowire. This model is derived from the solution of the Poisson equation to find channel potential using the dependence of depletion region under applied gate voltage. A good agreement was found when the results were compared with numerical simulation results of ATLAS platform.

In further work of Juan P. Duarte et. al. [31] a full range drain current model accumulation mode silicon nanowire transistor was proposed, with Pao-Sah electrostatic assumption and by extending the concept of parabolic potential approximation in the sub threshold and linear region including the dopant and mobile carrier charges. Based on the continuous charge model, the Pao-Sah integral is analytically solved to set a continuous drain current model. The proposed model is claimed to be appropriate for compact modeling, because it continuously captures the

phenomenon of the bulk conduction mechanism in all regions of device operation, including the subthreshold, linear and saturation regions.

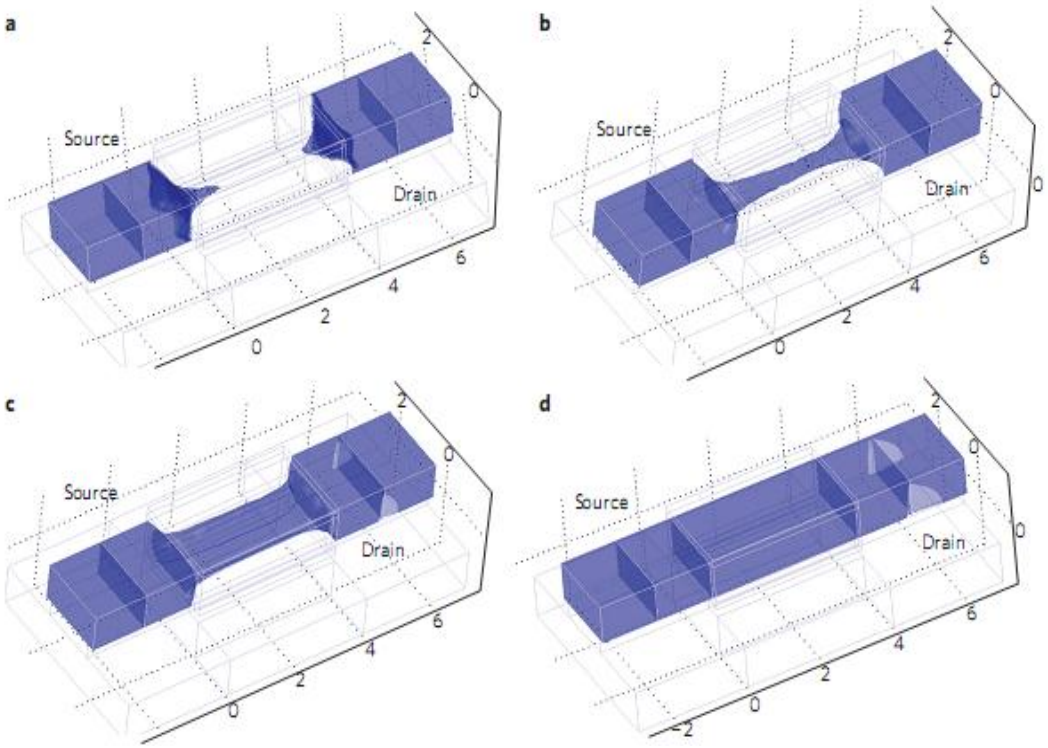


Figure 2.3: Electron concentration contour plots in an n-type accumulation mode silicon nanowire transistor. Plots are taken from simulations carried out for a drain voltage of 50 mV and for different gate voltages: below threshold ($V_G<V_{TH}$) the channel region is depleted of electrons (a); at threshold ($V_G = V_{TH}$) a string-shaped channel of neutral n-type silicon connects source and drain (b); above threshold ($V_G > V_{TH}$) the channel neutral n-type silicon expands in width and thickness (c); when a flat energy bands situation is reached ($V_G = V_{FB} >> V_{TH}$) the channel region has become a simple resistor (d). The plots were generated by solving the Poisson equation and the drift-diffusion and continuity equations self-consistently. The device has a channel width, height and length of 20, 10 and 40 nm, respectively. The n-type doping concentration is 1×10^{19} cm^{-3} (courtesy: Jean-Pierre Colinge et al. [10])

The probability of gate-all-around accumulation mode nanowire transistors using polycrystalline silicon was demonstrated by Chun-Jung Su et.al.[32] utilizing only one heavily doped poly-Si NW to serve as source, channel and drain region. In this work it was found that the fabricated gate-all-around polycrystalline nanowire transistors with a NW thickness 12 nm exhibited excellent I_{on}/I_{off} ratio of 5.2×10^{6}, quite a good sub- threshold slop of 199mV/dec being a polysilicon device, enhanced drive current as well as good immunity to short channel effects. It is also observed that this device exhibited lower source/drain series resistance than that its inversion-mode counterpart.

2.2 Silicon NW Bio-sensor

While transistor behavior of simple silicon nanowire is interesting as a disruptive switching device it has quite a promising application as biosensors. A typical nanowire biosensor can be a single or an array of nanowires which is laid on an insulator between source and drain [Fig. 2.4]. Electrodes of these source and drain are isolated by a protection layer. On Si-NW surface, target receptors which have the capability of immobilizing the targets, e.g. ions, DNA, proteins are attached by molecular linkers. Due to large surface to volume ratio, the charges associated with the attached molecules can deplete or accumulate entire cross sectional path way. And hence NW conductance gets easily changed. This phenomenon resulted in the most promising breakthrough in the 21th century by possible application of simple NW devices for disease diagnosis.

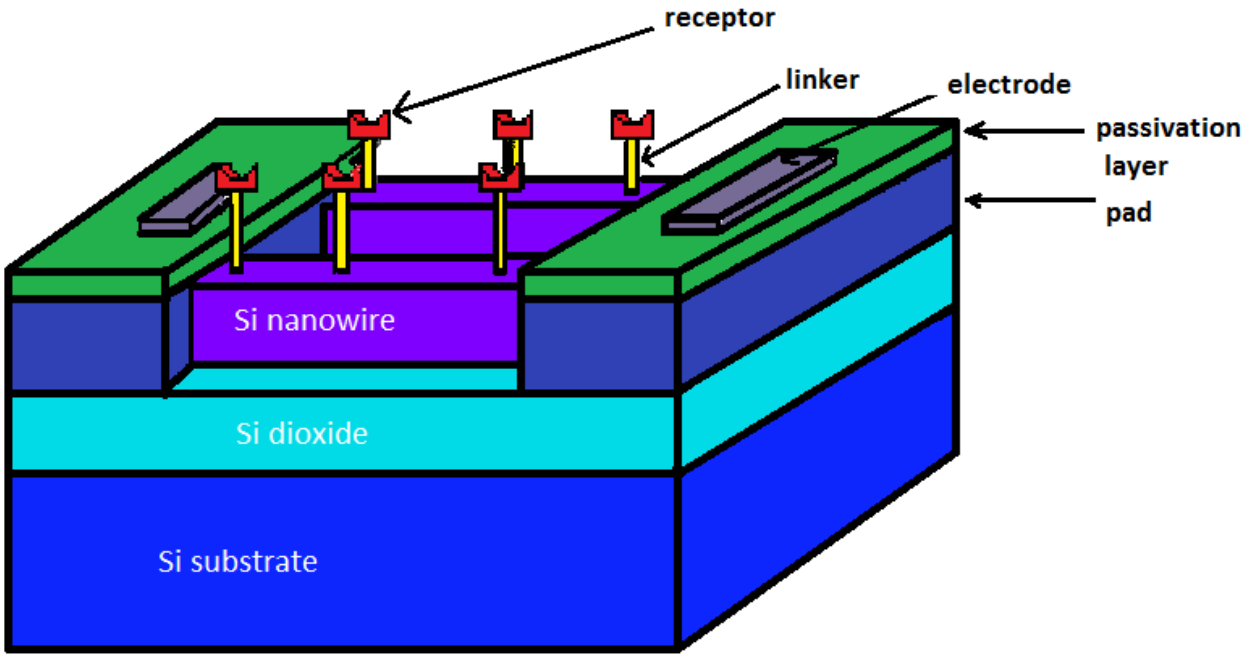


Figure 2.4: Schematic diagram of the structure of Si-NW biosensor

Table 2.1 shows a simple survey of silicon nanowire / nanoribons which have been used as biosensor. From this table, it is evidence that quite a broad range nanowire thicknesses and doping are employed for biosensor fabrication. This was mainly due to the experimental constraints of bottom up self-assembled nanowire fabrication where doping was achieved as well in a self-assembled nature by gas flow adjustment. In top down method at doping was incorporated a bit arbitrarily as no information of required doping for any particular thickness was available. It is worth mentioning that low doped nanowires were expected to be highly sensitive as low gate voltages can easily deplete or accumulate nanowires. However, low doped nanowires also become highly sensitive to environmental change which is difficult for viable biosensing application as signals due to biomolecules are easily get mixed up with signals generated from environmental change like moisture, presence of gaseous molecules etc.

Table 2.1: Survey of Si nanowire/nanoribbon biosensors

Year	Nanowires	Lithography[a]	Doping/Dose/ resistivity/sheet resistance	NW Thickness	Detection limit	Ref.
2006	SOI[b], n-&p-type, pass[c] :Si_3N_4	e-beam[d] -	~$10^{19}cm^{-3}$	20nm	1 nM 10 pM	[18]
2007	SOI, n-&p-type	DUV[e]	10^{13} to10^{15} cm^{-2}	40nm	10 pM	[26]
2008	SOI,p-type	e-beam	14–22 Ω cm	100nm	1 nM	[21]
2008	SOI,p-type	e-beam	$10^{18}cm^{-3}$	100nm	1 μM	[22]
2009	SOI,n-type	DUV	5*10^{13} cm^{-2}	~80nm	1 fg/mL	[20]
2009	Poly-Si, n-type	e-beam	40–50 Ω/ cm^2	80nm	10 nM	[27]
2010	Poly-Si, n-type	e-beam	40–50 Ω/ cm^2	80nm	30 nM	[19]
2012	Poly-Si, p-type	Spacer etch	~10^{16} cm^{-3}	100nm	10 fM	[28]

a: lithography only refers to the lithography techniques for nanowires patterning, whilst optical photolithography might be used throughout other processes.

b: SOI- silicon on insulator

c: passivation layer to isolate device from analyte

d: e-beam-electron-beam lithography

e: DUV – deep-ultraviolet lithography

In this work, we first time investigate accumulation mode silicon nanowire transistor behavior for nanowire thicknesses ranging from 5nm to 100nm with doping density diverging from $10^{14}cm^{-3}$ to 10^{20} cm^{-3} to find out the required doping for onset of transistor action at any particular thickness.

CHAPTER 3: METHODOLOGY

3.1 Device features and simulation models

The investigation of accumulation mode silicon nanowire transistors were done with the help of numerical simulations using the Silvaco Atlas device simulator [33], installed on a VLSI lab of East West University. A p-type silicon nanowire transistor with 1µm channel length was created on 500 nm oxide substrate (Fig. 3.1) and was simulated for different NW thicknesses and doping. The gate oxide thickness was 2 nm and the heavily doped poly-silicon layer of 1 µm length was used as gate material. In the silicon nanowire, two heavily doped regions on the two sides of the channel were employed to ensure ohmic contacts on the source/drain regions. The gate doping was $10^{21}/cm^3$ and the source/drain regions were also heavily doped with doping density of 1×10^{21} cm^{-3}. The channel doping was varied from $10^{14}/cm^3$ to $10^{20}/cm^3$ for analysis. Here, the gate doping was n-type whereas source, drain and channel doping was p-type. To contact source, drain and gate aluminum electrode of 50nm width was chosen.

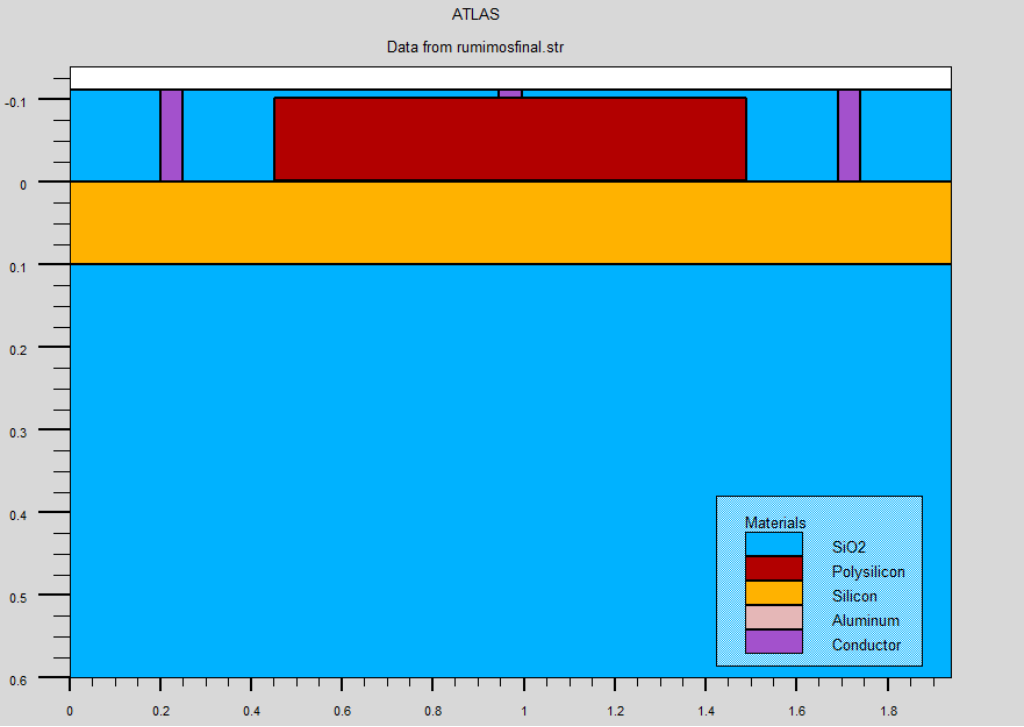


Figure 3.1: Schematic of the simulated p-type silicon nanowire transistor.

Lombardi (CVT) model was used to take account temperature (T_L), perpendicular electric field ($E_\perp$), parallel electric field (E//) and doping concentration (N) effects [33]. This model surpasses any other mobility models. In the CVT model, the transverse field, doping dependent and temperature dependent parts of the mobility are given by three components that are combined using Mathiessen's rule. These components are surface mobility limited by scattering with acoustic phonons (μ_{AC}), the mobility limited by surface roughness (μ_{sr}) and the mobility limited by scattering with optical intervalley phonons (μ_b) are combined using Mathiessen's rule as follows [33]:

$$\mu_T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{sr}^{-1} \qquad (3.1)$$

The first component, surface mobility limited by scattering with acoustic phonons equations [33]:

$$\mu_{AC.n} = \frac{BN.CVT}{E_\perp} + \frac{CN.CVT\ N^{TAU.CVT}}{T_L E_\perp^{\frac{1}{3}}} \qquad (3.2)$$

$$\mu_{AC.p} = \frac{BP.CVT}{E_\perp} + \frac{CP.CVT\ N^{TAUP.CVT}}{T_L E_\perp^{\frac{1}{3}}} \qquad (3.3)$$

The equation parameters BN.CVT, BP.CVT, CN.CVT, CP.CVT, TAUN.CVT, and TAUP.CVT used for this simulation are shown in Table 3-1 [32].

The second component, surface roughness factor is given by [33]:

$$\mu_{sr} = \frac{DELN.CVT}{E_\perp^2} \qquad (3.4)$$

$$\mu_{sr} = \frac{DELP.CVT}{E_\perp^2} \qquad (3.5)$$

The equation parameters DELN.CVT and DELP.CVT used for this simulation are shown in Table 3.1 [33].

The third mobility component, mobility limited by scattering with optical intervalley phonons is given by [33]:

$$\mu_{b.n} = MU0N.CVT \exp\left(\frac{-PCN.CVT}{N}\right) + \frac{\left[MUMAXN.CVT\left(\frac{T_L}{300}\right)^{-GAMN.CVT} - MU0N.CVT\right]}{1+\left(\frac{N}{CRN.CVT}\right)^{ALPHN.CVT}} - \frac{MU1N.CVT}{1+\left(\frac{CSN.CVT}{N}\right)^{BETAN.CVT}} \qquad (3.7)$$

$$\mu_{b.p} = MU0P.CVT \exp\left(\frac{-PCP.CVT}{N}\right) + \frac{\left[MUMAXP.CVT\left(\frac{T_L}{300}\right)^{-GAMP.CVT} - MU0P.CVT\right]}{1+\left(\frac{N}{CRP.CVT}\right)^{ALPHP.CVT}} - \frac{MU1N.CVT}{1+\left(\frac{CSP.CVT}{N}\right)^{BETAP.CVT}} \qquad (3.8)$$

Table 3.1: Parameters for Equations 3.1 to 3.8

Statement	Parameter	Default	Units
MOBILITY	BN.CVT	4.75×10^{7}	cm/ (a)
MOBILITY	BP.CVT	9.925×10^{4}	cm/ (a)
MOBILITY	CN.CVT	1.74×10^{5}	
MOBILITY	CP.CVT	8.842×10^{5}	
MOBILITY	TAUN.CVT	0.125	
MOBILITY	TAUP.CVT	0.0317	
MOBILITY	GAMN.CVT	2.5	
MOBILITY	GAMP.CVT	2.2	
MOBILITY	MUON.CVT	52.2	cm^2/ (v-a)
MOBILITY	MUOP.CVT	44.9	cm^2/ (v-a)
MOBILITY	MU1N.CVT	43.4	cm^2/ (v-a)
MOBILITY	MU1P.CVT	29.0	cm^2/ (v-a)
MOBILITY	MUMAXN.CVT	1417.0	cm^2/ (v-a)
MOBILITY	MUMAXP.CVT	470.5	cm^2/ (v-a)
MOBILITY	CRN.CVT	9.68×10^{14}	cm^{-3}
MOBILITY	CRP.CVT	2.23×10^{17}	cm^{-3}
MOBILITY	CSN.CVT	3.43×10^{20}	cm^{-3}
MOBILITY	CSP.CVT	6.10×10^{20}	cm^{-3}
MOBILITY	ALPHN.CVT	0.680	
MOBILITY	ALPHP.CVT	0.71	
MOBILITY	BETAN.CVT	2.00	
MOBILITY	BETAP.CVT	2.00	
MOBILITY	PCN.CVT	0.0	cm^{-3}
MOBILITY	PCP.CVT	0.23×10^{16}	cm^{-3}
MOBILITY	DELN.CVT	5.82×10^{14}	V/s
MOBILITY	DELP.CVT	2.054×10^{14}	V^2/s

The model for carrier emission and absorption processes proposed by Shockley-Read-Hall (SRH) was used to reflect the recombination phenomenon within the device. The electron and hole lifetimes τ_n and τ_p were modeled as concentration dependent. The equation is given by [33]:

$$R_{SRH} = \frac{pn - n_{ie}^2}{\tau_p\left[n + n_{ie}\exp\left(\frac{ETRAP}{kT_L}\right)\right] + \tau_n\left[p + n_{ie}\exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \quad (3.9)$$

$$\tau_n = \frac{TAUN0}{1 + \frac{N}{(NSRHN)}} \quad (3.10)$$

$$\tau_p = \frac{TAUP0}{1 + \frac{N}{(NSRHP)}} \quad (3.11)$$

where N is the local (total) impurity concentration. The used parameters TAUN0, TAUP0, NSRHN and NSRHP are Table 3-2 [33]. This model was activated with the CONSRH parameter of the MODELS statement.

Table 3.2: Default Parameters for Equations 3.9 to 3.11

Statement	Parameter	Default	Units
METERIAL	TAUNO	1.0×10^{-7}	s
METERIAL	NSRHN	5.0×10^{16}	cm^{-3}
METERIAL	TAUPO	1.0×10^{-7}	s
METERIAL	NSRHP	5.0×10^{16}	cm^{-3}

To account Bandgap narrowing effects, BGN model was used. These effects may be described by an analytic expression relating the variation in bandgap, ΔE_g, to the doping concentration, N. The expression used in ATLAS is from Slotboom and de Graaf [33]:

$$\Delta E_g = BGN.E\left\{ln\frac{N}{BGN.N} + \left[\left(ln\frac{N}{BGN.N}\right)^2 + BGN.C\right]^{\frac{1}{2}}\right\} \quad (3.12)$$

The used values for the parameters BGN.E, BGN.N and BGN.C are shown in Table 3.3 [33].

Table 3.3: Default parameters of Slotbooms Bandgap Narrowing Model for equation 3.12

Statement	Parameter	Default	Units
MATERIAL	BGM.E	9.0×10^{-3}	v
MATERIAL	BGN.N	1.0×10^{17}	cm^{-3}
MATERIAL	BGN.C	0.5	-

3.2 Simulation profile

Device simulation using silvaco atlas usually faces convergence problems and necessitates long run times. For this reason, the simulation of the accumulation mode silicon nanowire MOSFET has been divided into a few groups. Firstly, Structure definition was performed. In this definition the simulation focused on creating the structure with a suitable mesh density. Regions and electrodes were defined as depicted in Fig. 3.2. Finer nodes were assigned in critical areas, such as across the gate oxide for an accurate 2 nm thickness to monitor channel activity and near the source/drain boundaries to get a better picture of the depletion layer and junction behavior. A coarser mesh was used elsewhere in order to reduce simulation run time.

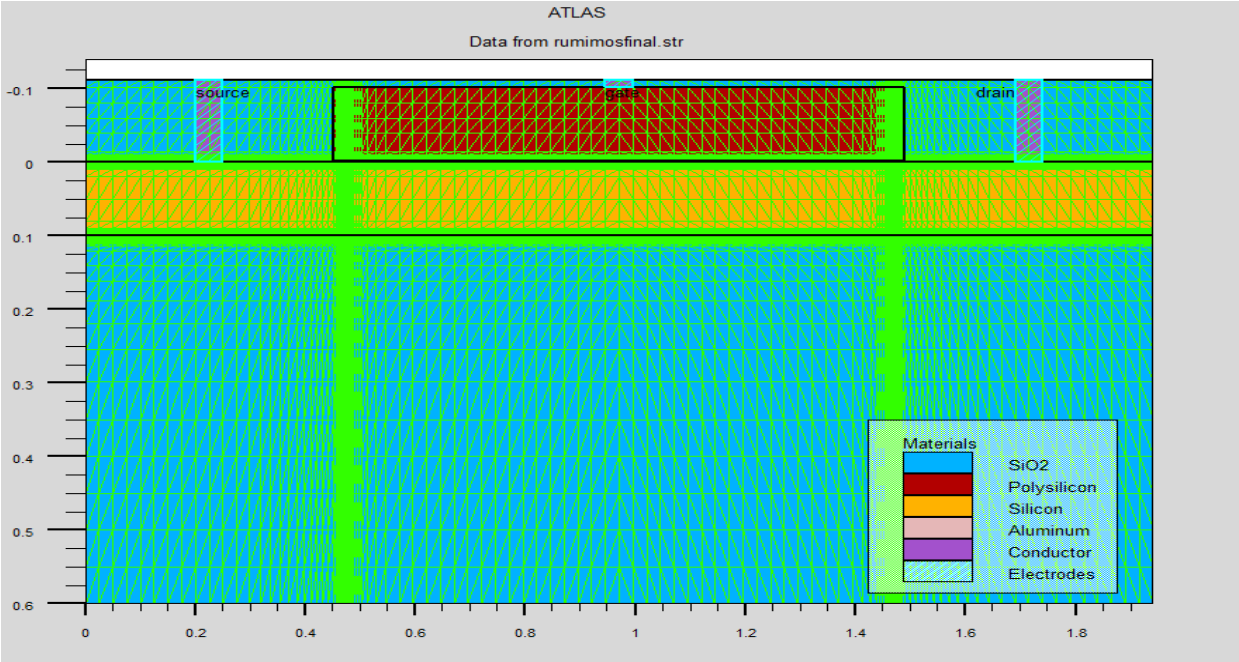


Figure 3.2: Cross-sectional view of p-type nanowire transistor showing the mesh density used in this simulation.

Once the structure and the mesh were satisfactory, the simulation was performed with appropriate models as discussed in section 3.1 and numerical solving methods. The models were invoked by using the statements FERMI, CVT, CONSRH, BGN. The numerical solving methods GUMMEL, NEWTON were used to reduce the simulation run time, while keeping the accuracy of the simulation at a tolerable level.

To get convergence, a special bias point solving method was used. It was found that the simulation faced difficulty in solving at the initial desired bias points, i.e. 0.5 V, 1 V, 1.5 V and 2 V for drain voltage and 0 V, - 0.5 V, -1 V,-1.5 V ,-2 V, -2.5 V and -3 V for gate voltage . Hence, the initial drain bias was set to 0.005 V and the next bias point was set to 0.05 V, before finally setting the bias point to desired value. For each biasing point a curve was generated for Vg varying from 5 V to -5 V with decrement 0.025 V and vd varying from 0 V to -10 V with decrement 0.05 V.

CHAPTER 4: RESULTS

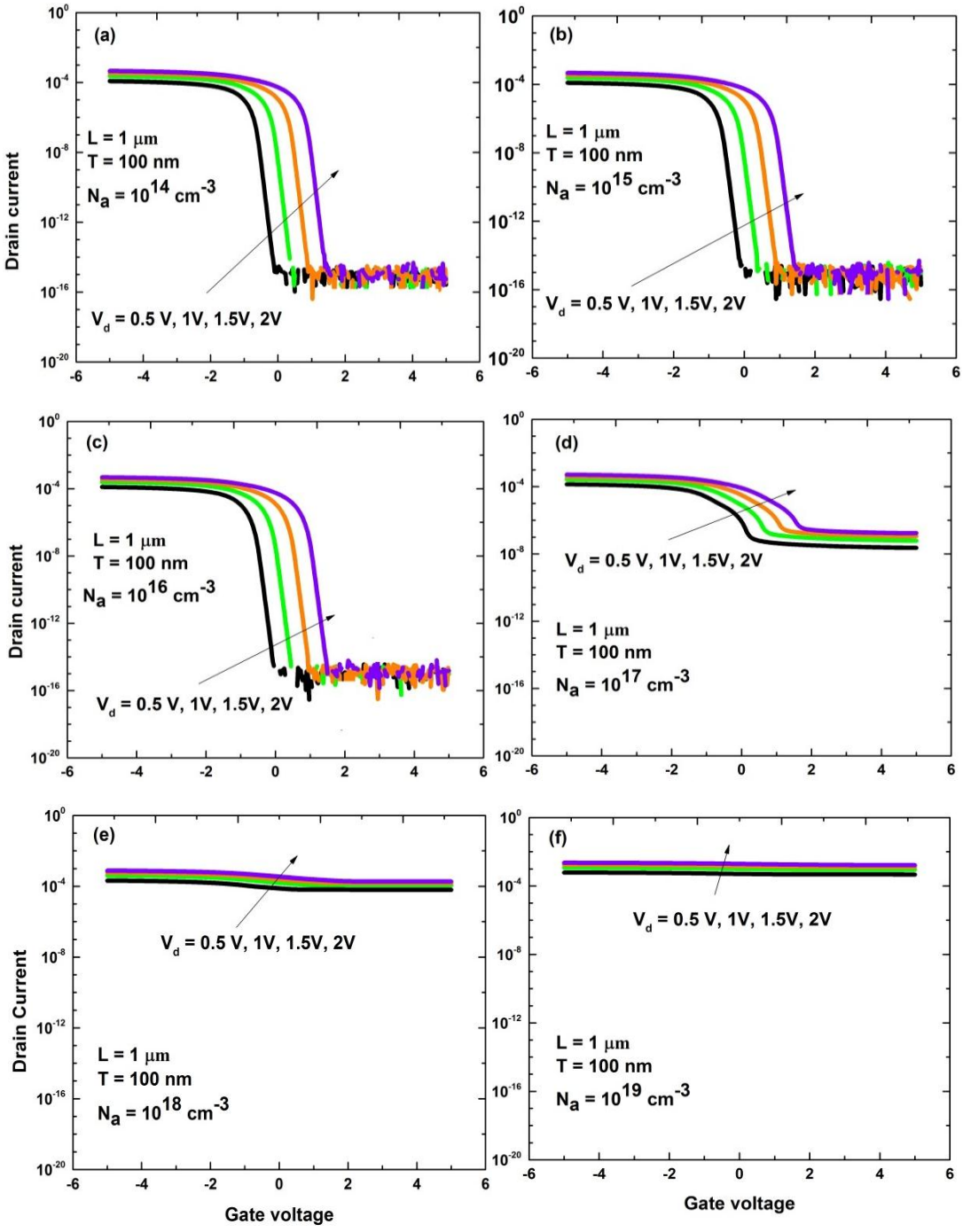


Fig. 4.1: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 100nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm (**Continued to next page**).

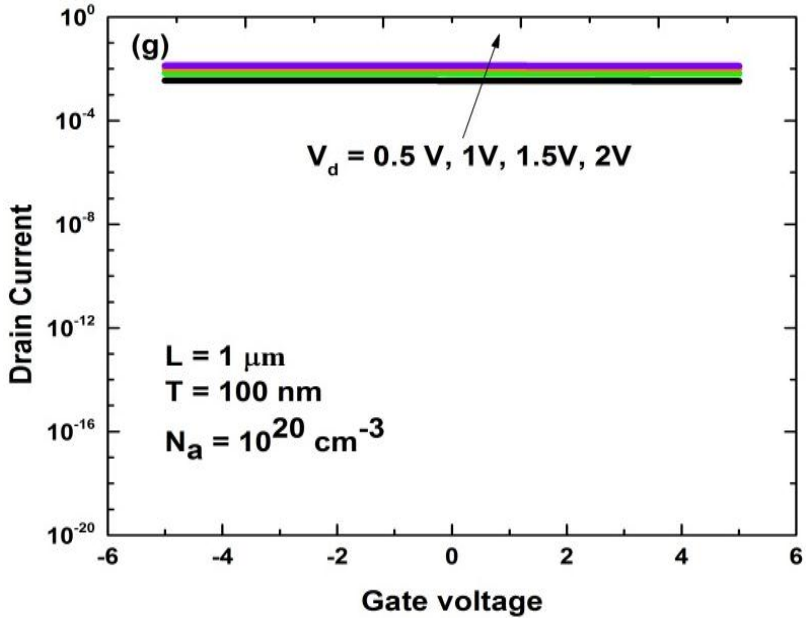


Fig. 4.1 (continued): Transfer characteristics (I_D vs V_G) of accumulation mode Si-NW transistors with NW thickness of 100nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm.

Fig. 4.1 shows the transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with a NW thickness of 100 nm and for different doping concentrations. For 100nm NW thickness, it can be observed that nanowires exhibit excellent transistor like behavior for doping concentration 10^{14} cm^{-3}, 10^{15} cm^{-3} and 10^{16} cm^{-3}(Fig. 4.1 (a), (b) and (c)) with sub- threshold slopes of 66.47 mv/decade, 66.47 mv/decade and 67.92 mv/decade at drain voltage of 0.5 V . At the doping concentration 10^{17} cm^{-3} (Fig. 4.1 (d)), the sub threshold slope is 777.33 mv/decade which implies quite a bad transistor behavior. At the doping concentration 10^{18} cm^{-3}, 10^{19} cm^{-3} and 10^{20} cm^{-3} (Fig. 4.1 (e), (f) and (g)), devices exhibit resistor like behavior rather than transistor.

Fig. 4.2 shows the transfer characteristics (I_D vs V_G) of accumulation mode Si-NW transistors with a NW thickness of 5 nm and for different doping concentrations. For 5 nm NW thickness, it is found that the nanowires exhibit quite a good transistor behavior for doping concentration 10^{14} cm^{-3}, 10^{15} cm^{-3} and 10^{16} cm^{-3} (Fig. 4.2 (a), (b) and (c)) with subthreshold slopes of 61.15 mv/decade, 61.15 mv/decade and 61.15 mv/decade which is similar to that of the 100nm NW thickness. However unlike 100nm thickness, Si-NW transistors with 5nm thickness also show excellent transistor behavior for doping concentrations of 10^{17} cm^{-3}, 10^{18} cm^{-3} and 10^{19} cm^{-3} with subthreshold slopes of 61.15 mv/decade, 61.92 mv/decade and 65.6 mv/decade (Fig. 4.2 (d), (e) and (f)). However, for 10^{20} cm^{-3} doping concentration 5nm Si NW transistor shows degraded transistor behavior with sub-threshold slope of 7552.3 mv/decade, which is preferable to accept as resistor like characteristics.

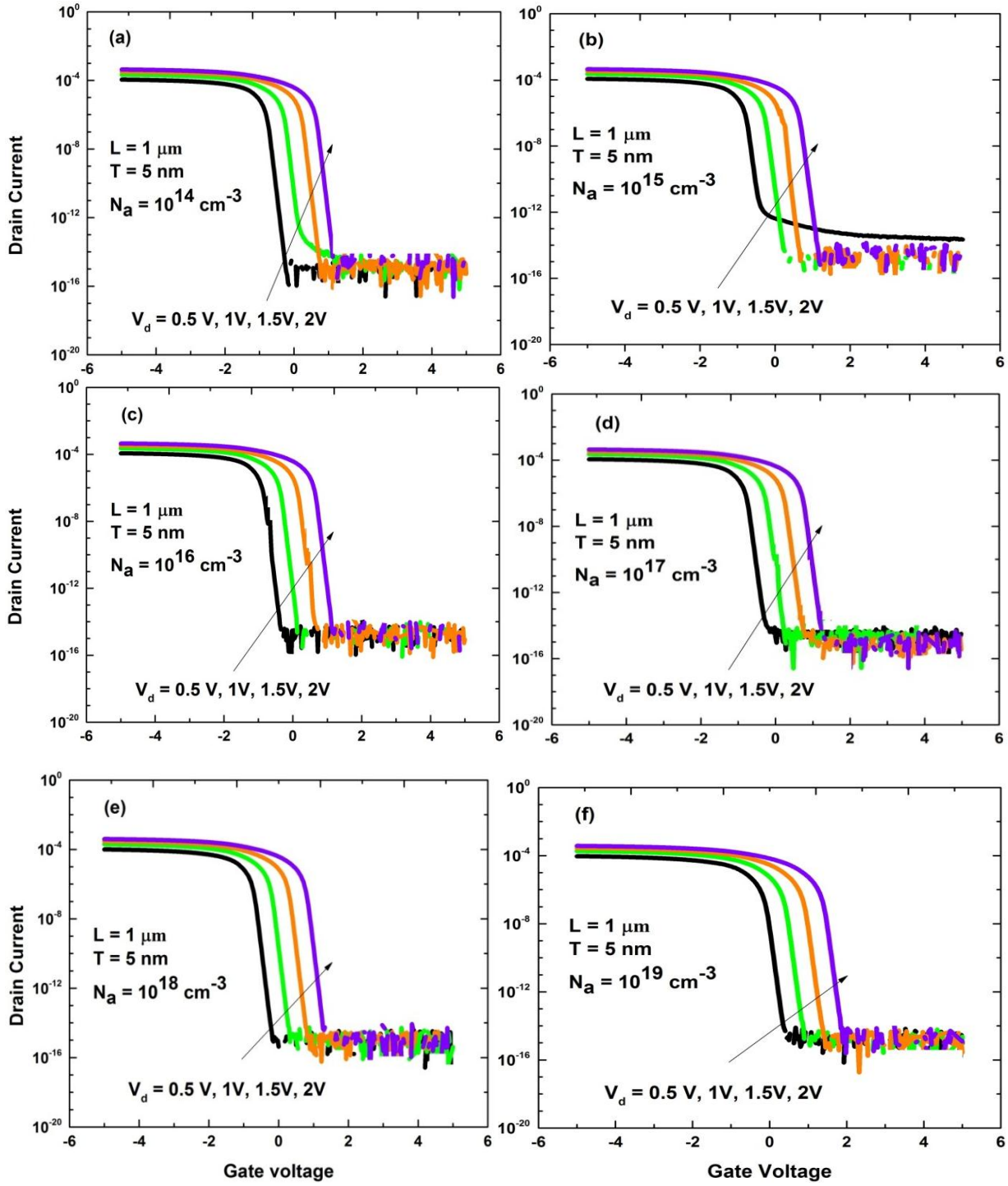


Fig. 4.2: Transfer characteristics (I_D vs V_G) of accumulation mode Si-NW transistors with NW thickness of 5nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm. (**Continued to next page**)

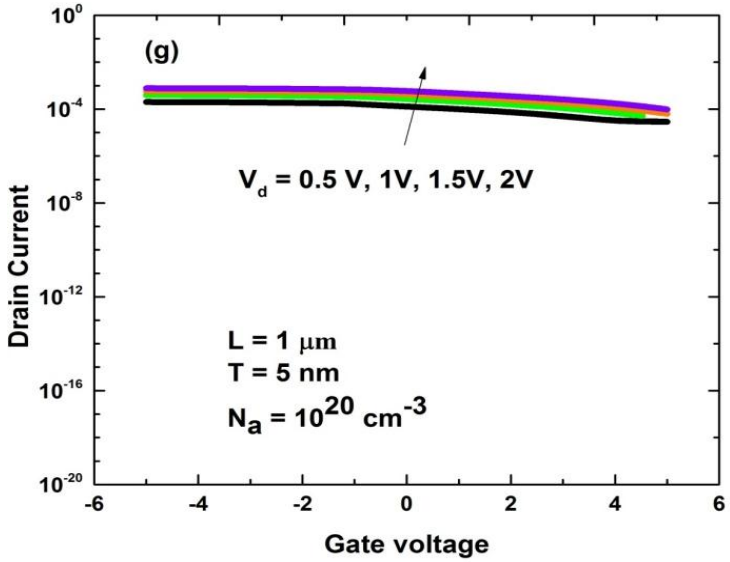


Fig. 4.2 (continued): Transfer characteristics (I_D vs V_G) of accumulation mode Si-NW transistors with NW thickness of 5nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm.

To characterize the NW behavior in more details, I_D vs V_d curves are generated for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. Fig. 4.3 shows the output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with a NW thickness of 100 nm and for different doping concentrations. It is seen that, for doping concentration of 10^{14} cm^{-3}, 10^{15} cm^{-3} and 10^{16} cm^{-3} (Fig. 4.3 (a), (b) & (c)) the drain currents show significant change with gate voltage which implies that in these doping concentrations, nanowires behave like transistors. In the doping concentration of 10^{17} cm^{-3} (Fig. 4.3 (d)), though a noticeable change in the drain current with gate voltage is found, actually at this doping concentration a weak transistor like behavior exists with a sub threshold slope of 777.33 mv/decade (Fig. 4.2 (d)) which is not readily visible in output characteristics of MOSFETs. In doping concentration 10^{18} cm^{-3} (Fig. 4.3 (e)) nanowire's drain current modulation with gate voltage is reduced, whereas in doping concentration 10^{19} cm^{-3} and 10^{20} cm^{-3}(Fig. 4.3 (f) & (g) no gate effect on the drain current is observed. These results indicate that 100 nm Si NW transistors show good transistor behavior for doping concentration of 10^{14} cm^{-3}, 10^{15} cm^{-3} and 10^{16} cm^{-3}. When doping concentration is increased from 10^{17} cm^{-3} to 10^{20} cm^{-3} Si NW gradually coverts from weak transistor to resistors due to the gradual loss of gate control. However, with the increase of the doping concentration from 10^{14} cm^{-3} to 10^{20} cm^{-3} the drain current of 100 nm Si NW's are increased for any particular V_D and V_G.

Fig. 4.4 shows the output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with a NW thickness of 5 nm and for different doping concentrations. It is observed that the drain currents show significant change with gate voltage for doping concentrations of 10^{14} cm^{-3}, 10^{15} cm^{-3} and 10^{16} cm^{-3} (Fig. 4.4 (a), (b) and (c)) which implies that in these doping concentrations, nanowires exhibit transistor action which is the similar behavior that is observed for 100nm NW thickness at these doping concentrations. However, unlike 100 nm Si NW thickness, 5 nm NWs

exhibiting excellent transistor behavior for doping concentrations of 10^{17} cm^{-3}, 10^{18} cm^{-3} and 10^{19} cm^{-3}. However, at doping concentration of 10^{20} cm^{-3} 5 nm Si NWs shows degraded transistor behavior which is similar to the observed in the output characteristics 100 nm Si NWs at the doping concentration of 10^{18} cm^{-3} (Fig. 4.3(e)).

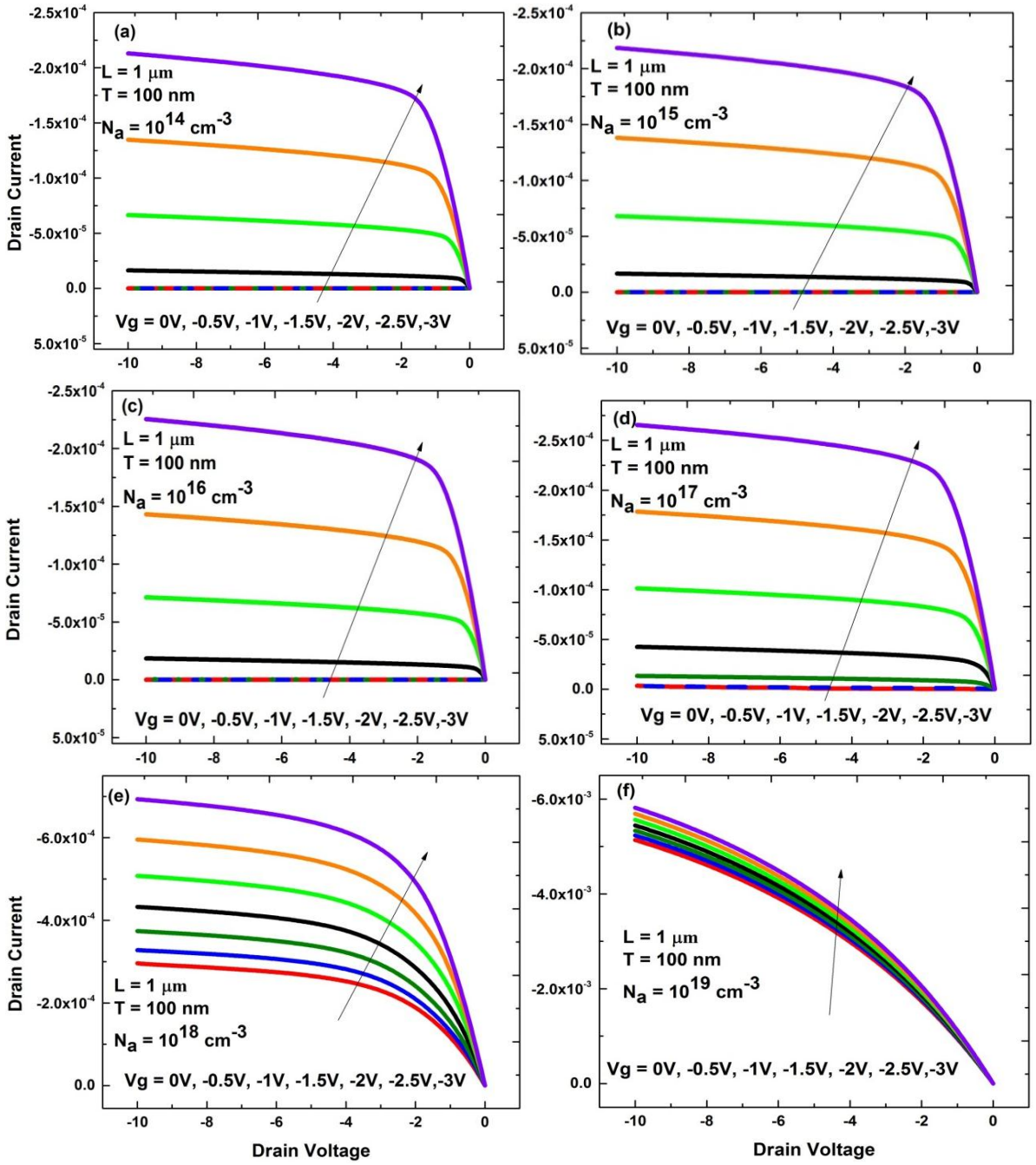


Fig. 4.3: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 100nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm. (**Continued to next page**).

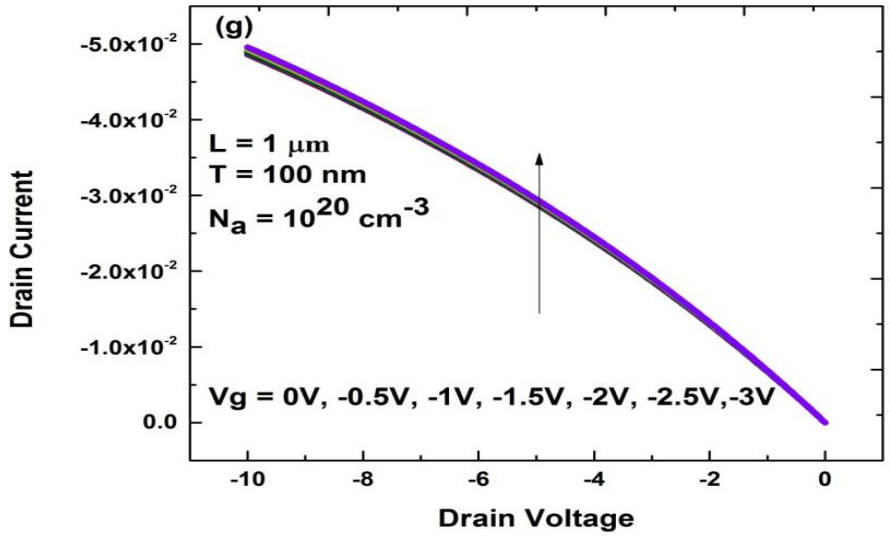


Fig. 4.3 (Continued): Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 100 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm.

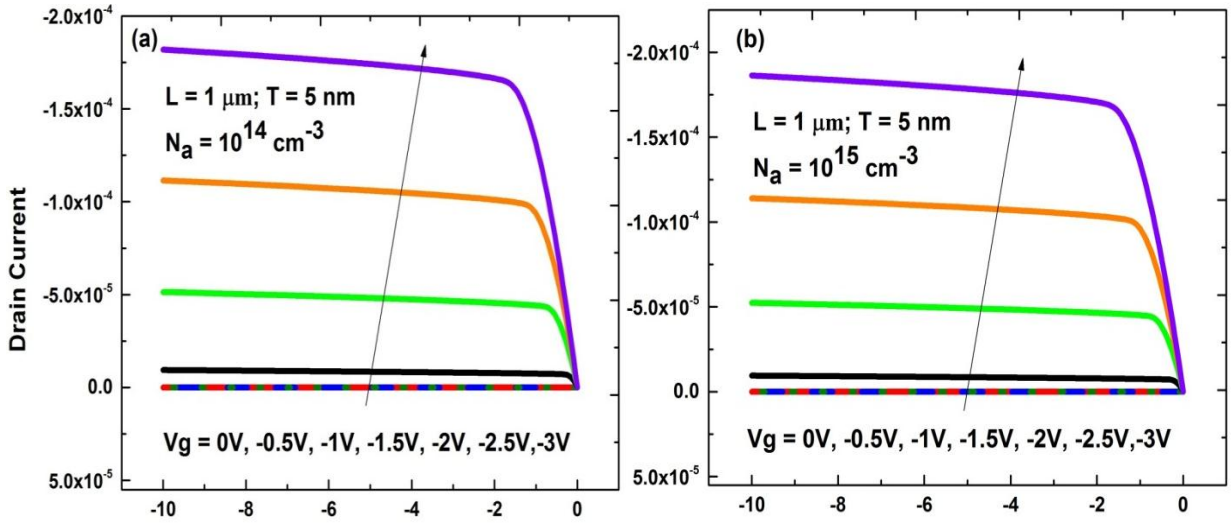


Fig. 4.4: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 5 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm. (**Continued to next page**).

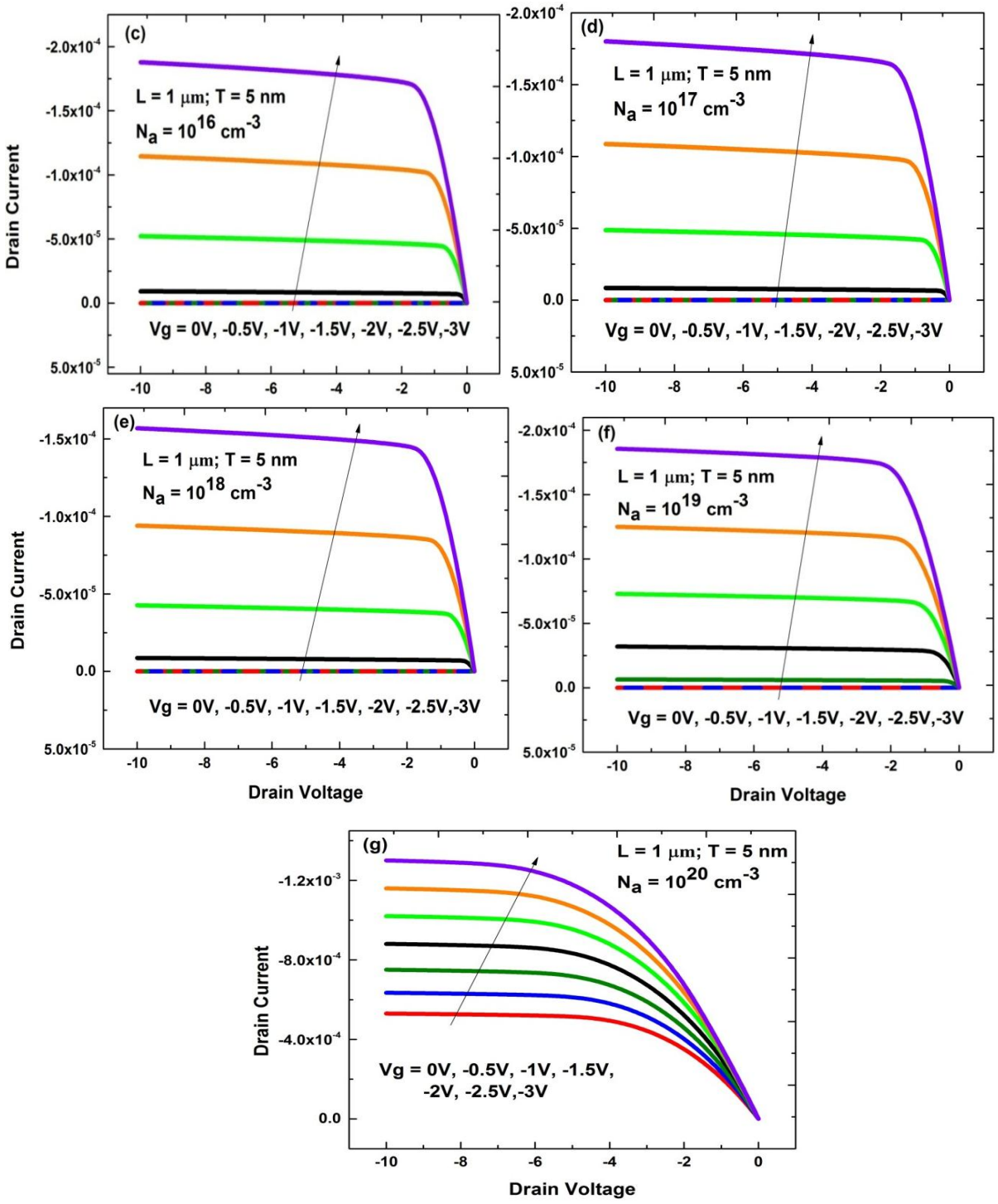


Fig. 4.4 (Continued): Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 5 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm.

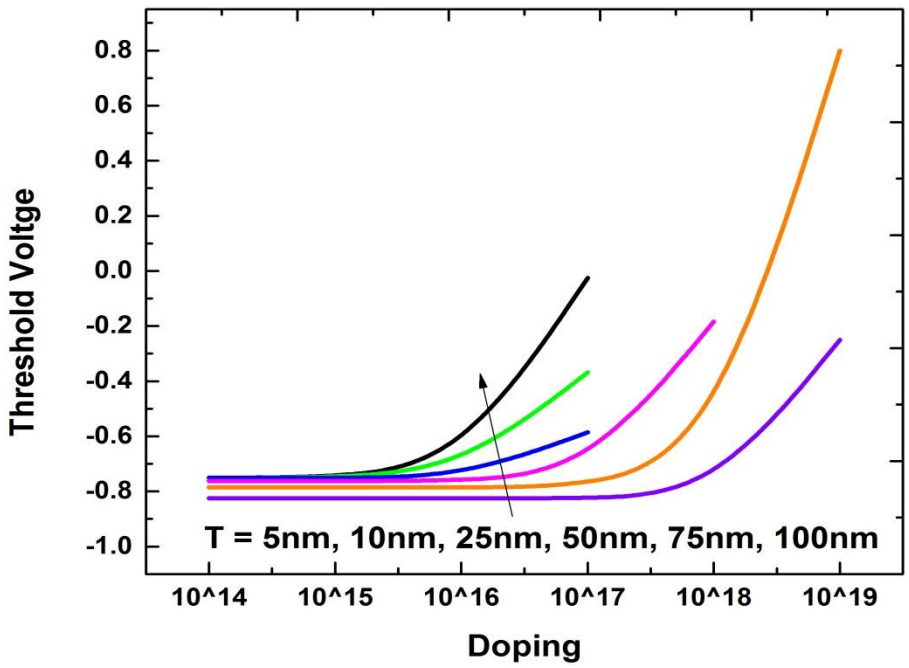
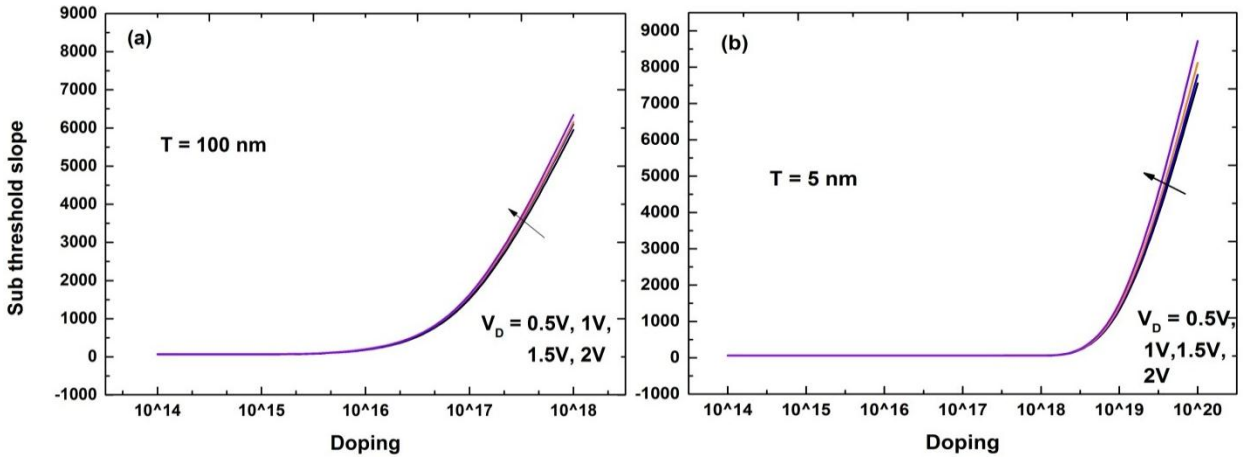


Fig. 4.5: Threshold voltage verses Doping for different NW thicknesses, i.e. 5nm, 10nm, 25nm, 50nm, 75nm and 100nm at drain voltage 0.5v. NWs have channel length of 1µm.

Fig. 4.5 shows threshold voltage as a function of doping for different NW thicknesses, i.e, 5nm, 10nm, 25nm, 50nm, 75nm and 100nm at drain voltage of 0.5v. For 100nm NW thickness, threshold voltages remain constant around -0.75v for doping concentrations of 10^{14} cm^{-3} , 10^{15} cm^{-3} and 10^{16} cm^{-3} while devices exhibit excellent transistor behavior (Fig. 4.1). At the doping density of 10^{17} cm^{-3} threshold voltage found to be -0.025 V implying that quite a less amount of accumulation is enough to reach threshold current. This can be attributed to the fact that for 100 nm NW thickness depletion strength is less for the doping density of 10^{17} cm^{-3} and hence, some conduction could occur within the body of the nanowire which also explains the bad transistor behavior of 100 nm NW at this doping (Fig. 4.2). Above 10^{17} cm^{-3} doping density no threshold voltage could be extracted for 100 nm NWs as devices behave as resistor rather than transistor (Fig. 4.1). For 5nm NW thickness, threshold voltages are around -0.8 V for doping concentrations of 10^{14} cm^{-3} , 10^{15} cm^{-3}, 10^{16} cm^{-3}, 10^{17} cm^{-3} and 10^{18} cm^{-3} and devices again exhibit excellent transistor behavior (Fig. 4.2). Although for doping density of 10^{19} cm^{-3} 5 nm nanowires exhibiting a less negative threshold voltage of -0.25v and hence, the device required less accumulation to reach threshold current, it is still exhibiting good transistor behavior due to high volume constriction of 5 nm thick NW. In general Fig. 4.5 also shows that with decreasing NW thicknesses threshold voltages of NWs at different doping density is becoming more negative which can be easily understandable as thin NWs have more constricted volume and hence, strong affect of depletion thereby requiring strong negative potential to reach threshold current.



4.6: Sub threshold slope verses Doping for NW thicknesses a) 100nm and b) 5nm. NWs have channel length of 1µm.

Fig. 4.6 shows sub threshold slopes as a function of doping at different drain voltages i.e, 0.5 V, 1 V, 1.5 V and 2 V for NW thicknesses of (a) 100nm and (b) 5nm. For 100nm NW thickness in Fig. 4.6 (a), sub-threshold slope is found to be around 67 mV/decade for doping concentrations of 10^{14} cm^{-3}, 10^{15} cm^{-3} and 10^{16} cm^{-3} for drain voltages of 0.5 V, 1 V, 1.5 V and 2 V. At these doping densities 100 nm Si NW exhibits excellent transistor behavior (Fig. 4.1) and the interesting phenomenon is that no degradation of sub-threshold slope could be observed with increasing drain bias in accumulation mode Si NW transistors like conventional inversion mode MOSFETs. However above these doping densities, 100 nm accumulation mode Si NW transistors gradually exhibit weak transistors to resistor like behavior and slight degradation in the sub-threshold slopes can be observed with increasing drain bias. For 5nm NW thickness in Fig. 4.6 (b), sub-threshold slope is found to be around 61 mV/decade for doping concentrations of 10^{14} cm^{-3} to 10^{19} cm^{-3} for all drain voltages of 0.5 V, 1 V, 1.5 V and 2 V. Again at these doping densities while 5 nm Si NW exhibiting excellent transistor behavior (Fig. 4.2) no degradation of sub-threshold slope could be observed with increasing drain bias in accumulation mode Si NW transistors. Similar behavior is observed in the sub-threshold characteristics for other NW thicknesses.

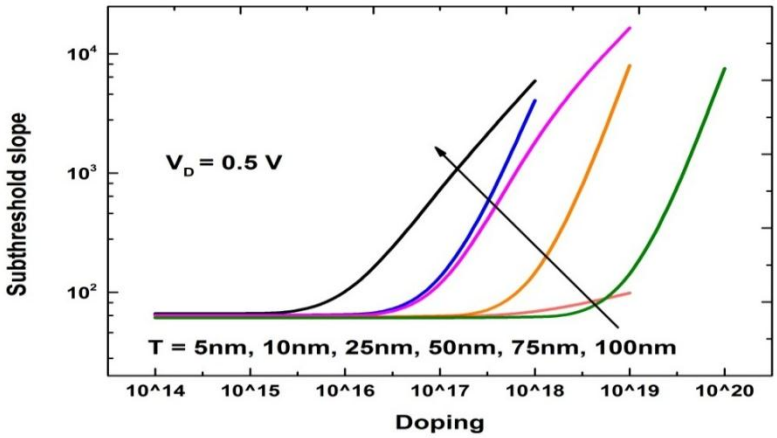


Fig. 4.7: sub threshold slope verses Doping for different NW thicknesses, i.e. 5nm, 10nm, 25nm, 50nm, 75nm and 100nm at drain voltage 0.5 v. NWs have channel length of 1µm.

Fig. 4.7 shows sub-threshold slope as a function of doping for different NW thicknesses, i.e, 5nm, 10nm, 25nm, 50nm, 75nm and 100nm at drain voltage of 0.5v. For 100nm NW thickness, sub-threshold slopes are around 67 mv/decade for doping concentrations of 10^{14} cm^{-3} , 10^{15} cm^{-3}, and 10^{16} cm^{-3}. As discussed before, with increasing doping densities from 10^{17} cm^{-3} to 10^{18} cm^{-3} sub-threshold slope is gradually degraded in 100 nm accumulation mode Si NW transistors. For 5nm NW thickness, again sub-threshold slopes remain constant around 61 mv/decade for doping concentrations of 10^{14} cm^{-3} to 10^{19} cm^{-3} and at the doping density of 10^{20} cm^{-3} 5 nm Si NW accumulation mode transistor shows hardly any transistor action with a sub-threshold slope around 75552 mV/decade. However, it is worth noting that with the decrease of Si NW thicknesses sub-threshold slopes are gradually becoming more ideal for the doping densities while NWs are exhibiting transistor like behavior.

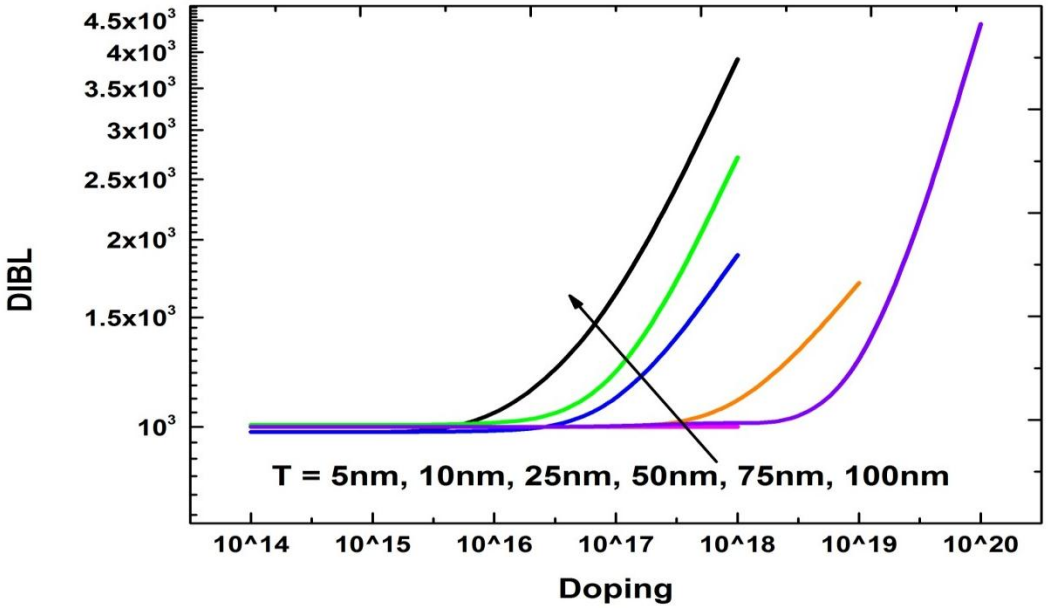


Fig. 4.8: DIBL verses Doping for different NW thicknesses, i.e. 5nm, 10nm, 25nm, 50nm, 75nm and 100nm.

Fig. 4.8 shows DIBL as a function of doping concentrations for different NW thicknesses, i.e, 5nm, 10nm, 25nm, 50nm, 75nm and 100nm. The DIBL behavior of accumulation mode NW transistors at different NW thicknesses and doping densities exhibit exactly similar behavior of threshold voltages and sub-threshold slopes as observed in Fig. 4.5 and Fig. 4.7 respectively. For example, at 100nm NW thickness DIBL value remain constant around 982 mv/v for doping concentrations of 10^{14} cm^{-3} , 10^{15} cm^{-3}, 10^{16} cm^{-3} whereas this parameter gets degraded to values 1500 mv/v and 3900 mv/v for doping concentrations of 10^{17} cm^{-3} and 10^{18} cm^{-3} when NW shows weak transistor or almost resistor like behavior. For 5nm NW thickness, DIBL values are almost similar to that of the 100 nm NW thickness with a value around 1000 mv/v for doping concentrations of 10^{14} cm^{-3} , 10^{15} cm^{-3}, 10^{16} cm^{-3}, 10^{17} cm^{-3}, 10^{18} cm^{-3} and 10^{19} cm^{-3}. Again at doping concentration of 10^{20} cm^{-3} 5 nm Si NW exhibit degraded value of 4440 mv/v. It is worth noting that while accumulation mode Si NW transistors exhibit plausible transistor action DIBL does not significantly change with NW thicknesses for the 1µm channel length NWs.

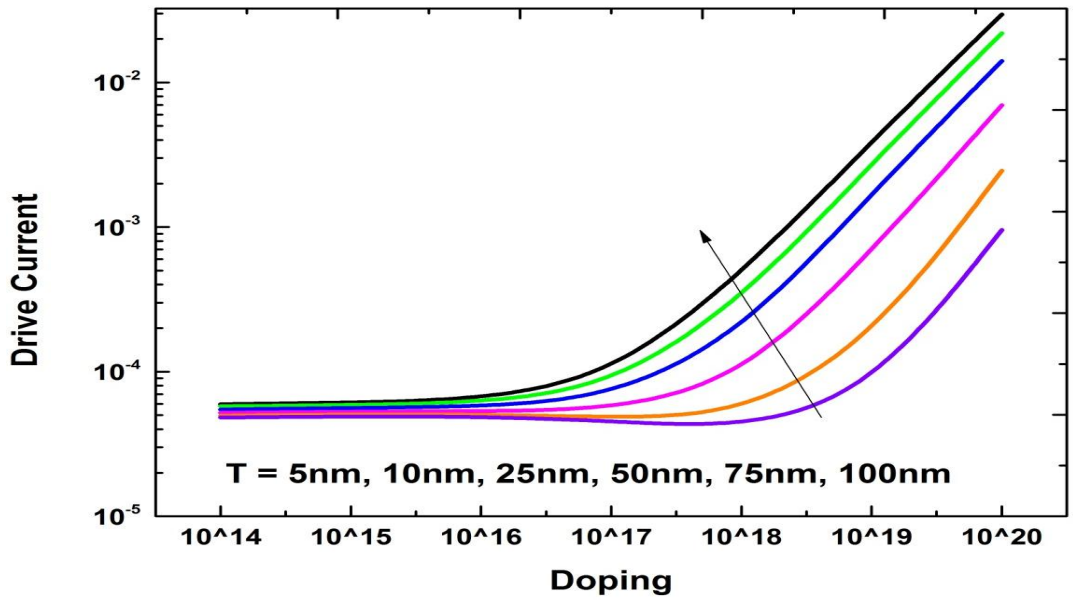


Fig. 4.9: Drive Current verses Doping for different NW thicknesses, i.e. 5nm, 10nm, 25nm, 50nm, 75nm and 100nm. NWs have channel length of 1µm.

Fig. 4.9 shows drive current as a function of doping for different NW thicknesses, i.e, 5nm, 10nm, 25nm, 50nm, 75nm and 100nm. In general drive current accumulation mode NW transistors decreases with the decrease of NW thicknesses at all doping densities which is a quite expected phenomenon due to the constriction of conduction volume. However, it is worth noting that the drive current reduction is quite significant in the doping concentrations when NWs either exhibit poor transistor action and/or resistor like behavior.

CHAPTER 5: DISCUSSION

The results of chapter 4 show that accumulation mode transistor behavior is strongly dependent on doping and NW thicknesses. For 100nm NW thickness, it is observed that nanowires exhibit excellent transistor like behavior for doping concentrations of 10^{14} cm^{-3} , 10^{15} cm^{-3}, 10^{16} cm^{-3}. An increase in the doping concentration into 10^{17} cm^{-3} or above gradually converts 100 nm Si NWs into weak transistor or simple resistors. For 5nm NW thickness, excellent transistor action is observed for a broad range of doping concentrations such as, 10^{14} cm^{-3} , 10^{15} cm^{-3}, 10^{16} cm^{-3}, 10^{17} cm^{-3}, 10^{18} cm^{-3} and 10^{19} cm^{-3}. Again at doping concentration of 10^{20} cm^{-3} 5 nm Si NW exhibit resistor like behavior. These results indicate that with the decrease of NW thicknesses Si NW works as accumulation mode transistor at significantly high level of doping concentrations.

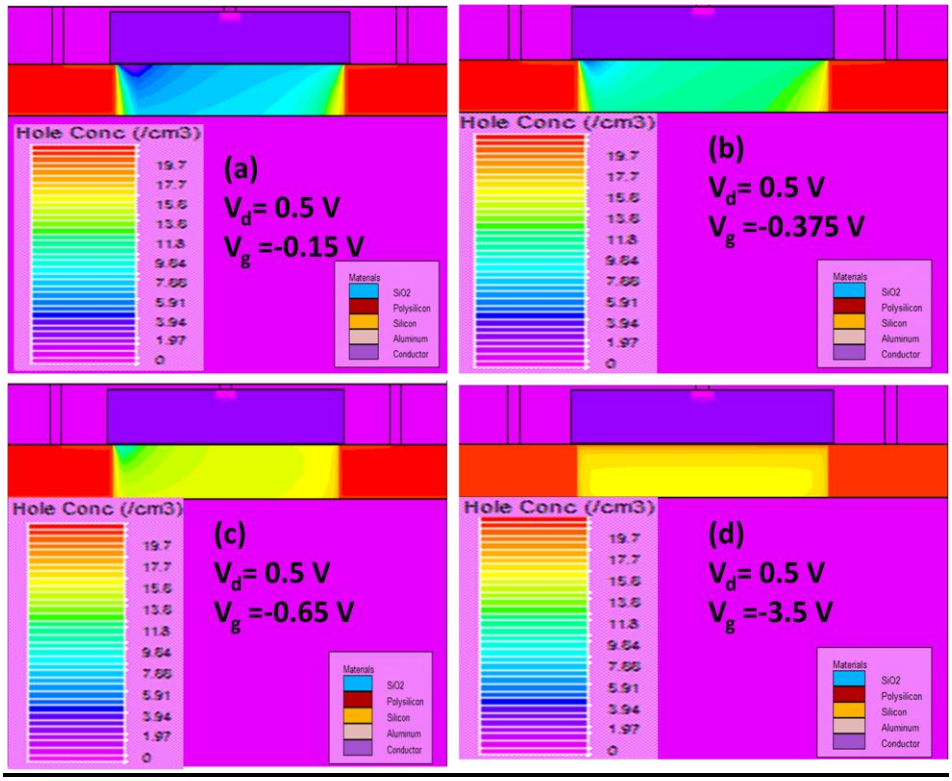


Fig. 5.1: Hole concentration contour plots of 100 nm Si NWs at different points of sub-threshold region for doping concentration of 10^{14} cm^{-3} and for V_d = 0.5V; a) At the bottom of the sub-threshold plot when the device is off with a V_g = -0.15V, b) at the middle part of the linear section of sub-threshold plot with a V_g = -0.375V, c) at the top part of the linear section of sub-threshold plot with a V_g = -0.65V (just before saturation) and d) at saturation with a V_g = -3.5V. 100 nm Si NWs at this doping concentration is exhibiting transistor like behavior.

To explain this phenomenon, Fig. 5.1 shows hole concentration contour plots of the 100 nm Si NW at different points of sub-threshold region for a doping concentration of 10^{14} cm^{-3} while 100 nm NW is behaving as an excellent transistors. At the bottom of the sub-threshold plot when the device is off with a V_g = -0.15V (Fig. 5.1 (a)), it can be seen that hole concentration varies from around 10^{3} cm^{-3} to 10^{6} cm^{-3} at the different regions of the channel. For a doping density of 10^{14}

cm^{-3} such amount of free holes is actually representing full depletion of the channel. At the middle part of the linear section of sub-threshold plot with a V_g = -0.375V (Fig. 5.1 (b)), hole concentrations are around 10^{12} cm^{-3} to 10^{13} cm^{-3} at the most of the sections of the channel. Such an amount of carrier concentrations represents mild accumulation. However, it is worth noting that accumulation is not uniform in the whole volume of the NW. Just before saturation with a V_g = -0.65V (Fig. 5.1(c)) increased accumulation can be seen with hole concentration varying from around 10^{14} cm^{-3} to 10^{16} cm^{-3} again with a non-uniform distribution along the volume of the NW channel. At saturation with a V_g = -3.5V (Fig. 5.1(d)), it can be seen that hole concentration varies from around 10^{16} cm^{-3} to 10^{17} cm^{-3} in the most of the region of the NW channel with better uniformity than Fig. 5.1 (a), (b) & (c). However, a thin layer with a hole concentration of around 10^{20} cm^{-3} can also be seen at the top region of the NW channel which is close to gate. This result indicate that with the increase of the negative gate bias, 100 nm NW with a doping density 10^{14} cm^{-3} gradually converts from depletion to partial accumulation to full accumulation of the channel volume. The transition from depletion to partial accumulation of the NW volume results in the linear section of the sub-threshold plot whereas the full accumulation of the volume results in the saturation of the drain current and hence, 100 nm Si NW with a doping concentration of 10^{14} cm^{-3} shows an excellent transistor behavior.

Fig. 5.2 shows hole concentration contour plots of 100 nm Si NWs at different gate voltages for doping concentration of 10^{19} cm^{-3} and for V_d = 0.5V. 100 nm thick Si NWs are exhibiting resistor like behavior at this doping concentration. At the V_g = -0.15V (Fig. 5.2 (a)), it can be observed that whole volume of the NW has a hole concentration of around 10^{19} cm^{-3} except for a tiny depletion region near the gate with a hole concentration around 10^{15} cm^{-3}. Similar behavior can be observed for V_g = -0.375V (Fig. 5.2 (b)), with a hole concentration of around 10^{19} cm^{-3} in the whole volume of the 100 nm NW. However, the tiny depletion region near the gate appears to be reduced at this gate voltage. For V_g = -0.65V and V_g = -3.5V (Fig. 5.2 (c) & (d)), no depletion region can be seen in the 100 nm NW but the whole volume remains conductive with a hole concentration around 10^{19} cm^{-3}. This result indicates that for 100 nm NW thickness with a doping concentration of 10^{19} cm^{-3}, there is no effect of gate voltages and quite a significant conduction path exists approximately through the whole volume of the NW at all gate voltages. As a result 100 nm thick NW at this doping density shows resistor like behavior.

To explain the transistor like behavior of 5 nm thick NW at the doping density of 10^{14} cm^{-3}, Fig. 5.3 shows hole concentration contour plots of 5 nm Si NWs at different points of sub-threshold region for doping concentration of 10^{14} cm^{-3} and for V_d = 0.5V. The behavior of 5 nm thick Si NW at this doping concentration (Fig. 5.3) is similar to the 100 nm thick Si NW at the doping density of 10^{14} cm^{-3}(Fig. 5.1). The hole concentration in the volume of the NW is found to be around 10^{7} cm^{-3} to 10^{9} cm^{-3}, 10^{11} cm^{-3} to 10^{13} cm^{-3}, 10^{14} cm^{-3} to 10^{17} cm^{-3} and 10^{18} cm^{-3} to 10^{20} cm^{-3} at gate voltages of -0.15V, -0.375V, -0.65V and -3.5V respectively. This result indicate that significant gate modulation exists for 5 nm NW with a doping density 10^{14} cm^{-3} and with the increase of negative gate bias NW volume gradually converts from depletion to partial accumulation to full accumulation explaining its transistor like behavior.

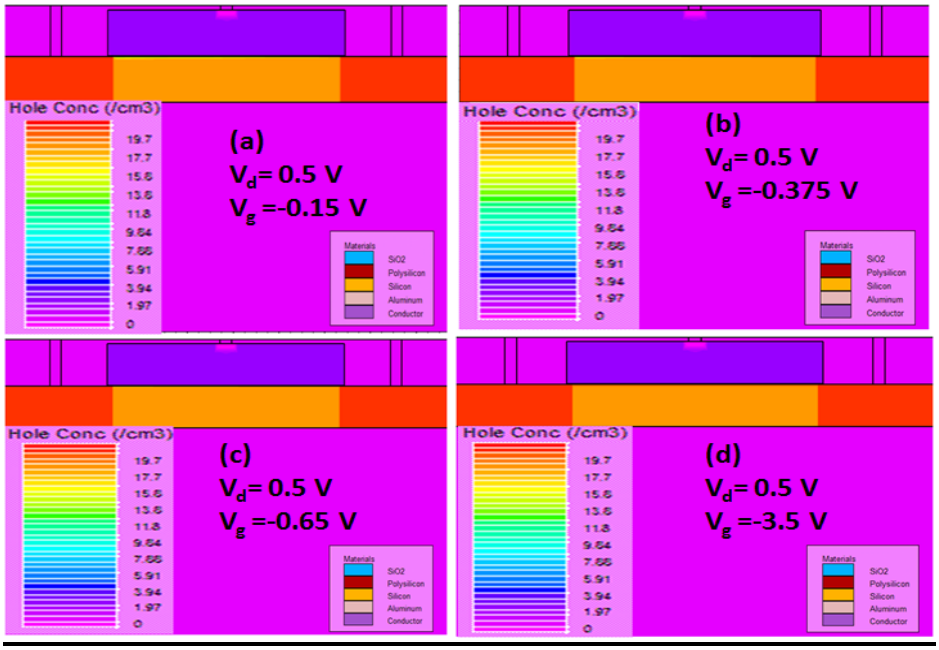


Fig. 5.2: Hole concentration contour plots of 100 nm Si NWs at different gate voltages for doping concentration of 10^{19} cm^{-3} and for V_d = 0.5V; a) for V_g = -0.15V, b) for V_g = -0.375V, c) for V_g = -0.65V and d) for V_g = -3.5V. 100 nm Si NWs at this doping concentration is exhibiting resistor like behavior.

Finally we explain transistor like behavior of 5 nm thick NW at the doping density of 10^{19} cm^{-3}. At this doping density 100 nm thick Si NW showed resistor like behavior rather than transistor action. Fig. 5.4 shows hole concentration contour plots of 5 nm Si NWs at different points of sub-threshold region for doping concentration of 10^{19} cm^{-3} and for V_d = 0.5V. Unlike 100 nm NWs where gate effect was observed in a tiny volume near the gate at this doping density (Fig. 5.2), 5 nm thick Si NW experienced a significant gate modulation all through its volume. The hole concentration in the volume of the 5 nm thick NW (Fig. 5.4) is found to be around 10^{12} cm^{-3} to 10^{15} cm^{-3}(with most of the volume at 10^{15} cm^{-3}), 10^{16} cm^{-3} to 10^{17} cm^{-3} (with most of the volume at 10^{16} cm^{-3}), 10^{16} cm^{-3} to 10^{17} cm^{-3} (with most of the volume at 10^{17} cm^{-3}) and 10^{19} cm^{-3} to 10^{20} cm^{-3} (with most of the volume at 10^{19} cm^{-3} and a flat region near the gate with 10^{20} cm^{-3}) at gate voltages of -0.15V, -0.375V, = -0.65V and -3.5V respectively. At the doping density of 10^{19} cm^{-3}, a tiny region is expected to be affected by gate. Significant volume constriction in the 5 nm thick NW appears to be sufficient for such modulation all through its volume and with the increase of negative gate bias 5 nm thick NW volume was able to be gradually converted from depletion to partial accumulation to full accumulation thereby explaining its transistor like behavior. Gate voltage modulation on a very small volume at the doping density of 10^{19} cm^{-3} also explains why 100 nm thick Si NW at this doping behaved as a resistor rather than transistor. These investigations (Fig. 5.1 to 5.4) also imply that with the increase of the doping density as the gate modulated volume is gradually decreasing, the whole volume can be affected only when NWs are thin and have constricted volumes and hence, thin NWs are able to exhibit transistor action at high doping density like 10^{19} cm^{-3} which is close to source/drain doping of conventional MOSFET. In contrast significant conduction path exists beyond the gate modulated volume of thick nanowires at high doping densities and hence, thick nanowires fail to show accumulation mode transistor action at high doping densities.

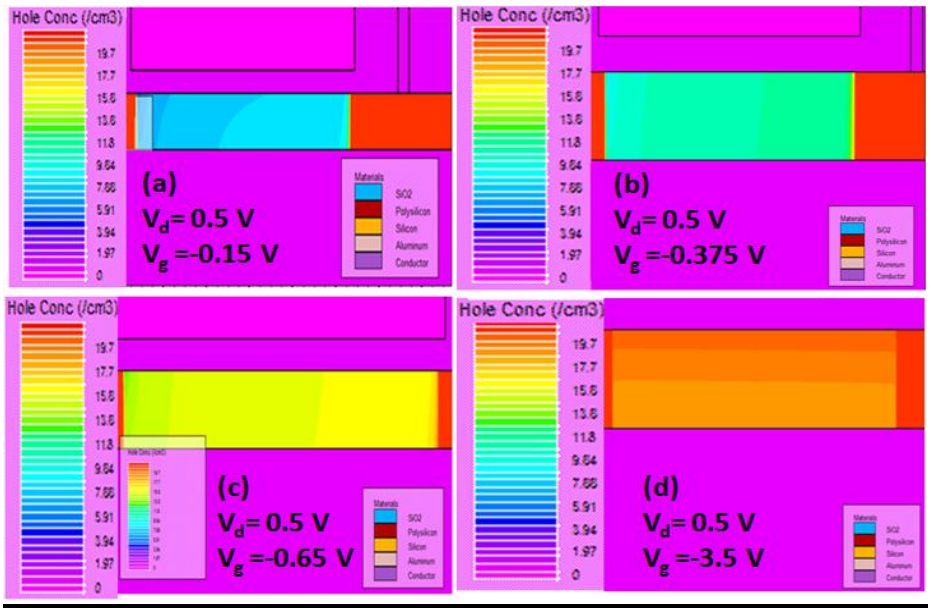


Fig. 5.3: Hole concentration contour plots of 5 nm Si NWs at different points of sub-threshold region for doping concentration of 10^{14} cm^{-3} and for V_d = 0.5V; a) At the bottom of the sub-threshold plot when the device is off with a V_g = -0.15V, b) at the middle part of the linear section of sub-threshold plot with a V_g = -0.375V, c) at the top part of the linear section of sub-threshold plot with a V_g = -0.65V (just before saturation) and d) at saturation with a V_g = -3.5V. 100 nm Si NWs at this doping concentration is exhibiting transistor like behavior.

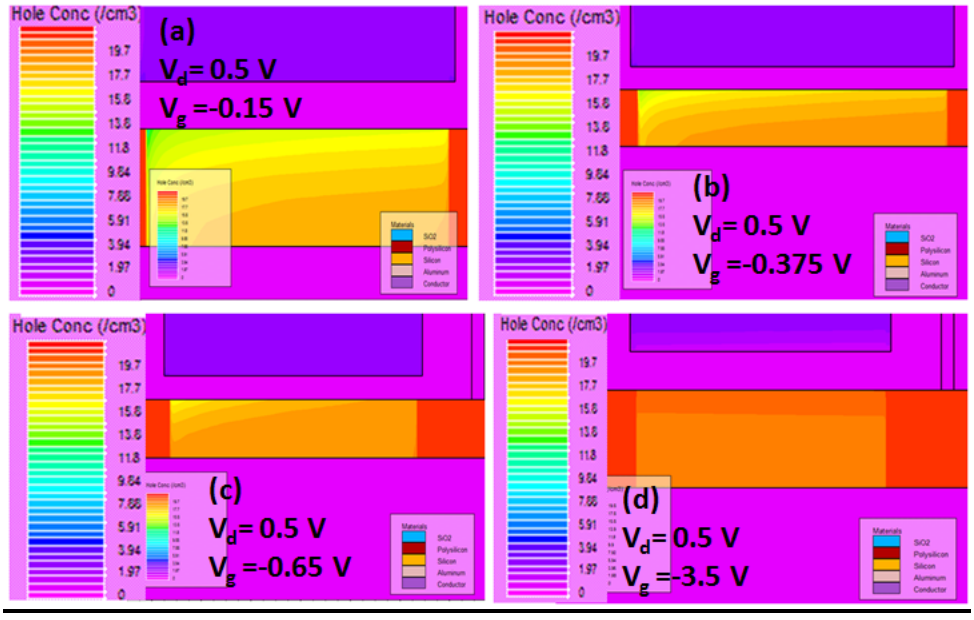


Fig. 5.4: Hole concentration contour plots of 5 nm Si NWs at different gate voltages for doping concentration of 10^{19} cm^{-3} and for V_d = 0.5V; a) for V_g = -0.15V, b) for V_g = -0.375V, c) for V_g = -0.65V and d) for V_g = -3.5V. 100 nm Si NWs at this doping concentration is exhibiting resistor like behavior.

CHAPTER 6: CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

We have investigated accumulation mode transistor behavior of p-type silicon nanowires at different doping concentrations and nanowire thicknesses to find out the relationship between NW thicknesses and doping for transistor action. The investigation is done for nanowire thicknesses ranging from 5 nm to 100 nm with doping density diverging from 10^{14}cm^{-3} to 10^{20} cm^{-3}. For 100 nm NW thickness, it is observed that nanowires exhibit excellent transistor like behavior for doping concentrations of 10^{14} cm^{-3}, 10^{15} cm^{-3}, 10^{16} cm^{-3}. An increase in the doping concentration into 10^{17} cm^{-3} or above gradually converts 100 nm Si NWs into weak transistor or simple resistors. For 5 nm NW thickness, it is found that the nanowires exhibit quite a good transistor behavior for doping concentration 10^{14} cm^{-3}, 10^{15} cm^{-3}, 10^{16} cm$^{-3,}$ 10^{17} cm^{-3}, 10^{18} cm^{-3} and 10^{19} cm^{-3}. However, for 10^{20} cm^{-3} doping concentration 5nm Si NW transistor again shows resistor like characteristics.

These results indicate that thick nanowire's transistor action is limited only at low doping concentrations whereas thin nanowires are able to exhibit transistor action at high doping densities even at 10^{19} cm^{-3} which is close to source/drain doping of conventional MOSFET. This phenomenon is explained by the gradually decreasing gate modulated volume in the NW with increasing doping concentrations. As a result, in thick NWs significant conduction path exists beyond the gate modulated volume at high doping densities and hence, thick nanowires fail to show accumulation mode transistor action at high doping densities. In thin nanowires, significant volume constriction ensures that the whole constricted volume to be affected by gate voltage and hence, thin nanowires are able to show transistor action at high doping densities. For a good bio-sensing application, large change in NW conductance upon attachment of biomolecules is needed and hence, transistor behavior of nanowires is somehow imperative for biosensors. A good transistor behavior of Si NW is also very important for accumulation mode junction less NW transistor fabrication if switching is targeted. The following table summarizes the result of this research showing the silicon NW thicknesses and doping window for bio-sensing application and junction less NW transistor fabrication.

Table 6.1: Silicon nanowire thicknesses and doping window for biosensors

No	NW thicknesses	Required doping
1	100 nm	$\leq 10^{16}/cm^3$
2	75 nm	$\leq 10^{17}/cm^3$
3	50 nm	$\leq 10^{17}/cm^3$
4	25 nm	$\leq 10^{18}/cm^3$
5	10 nm	$\leq 10^{18}/cm^3$
6	5 nm	$\leq 10^{19}/cm^3$

6.2 Future work

- This simulation is done using default parameter values for silicon in ATLAS framework without taking into account of any interface states and/or surface roughness in silicon nanowires to understand the behavior of accumulation mode NW transistors. In future, interface states will be incorporated and the results will be calibrated with experiment to get more physical understanding of the trend.

- The simulation is done with gate effect just from one side. 3D simulation will be done in future to get the real picture of surround gate effects.

- Simulated accumulation mode nanowires have channel length of one micron with heavily doped p+ regions at source and drain. In future effect of channel length on the accumulation mode nanowire transistors will be done with varying channel lengths both with heavily doped source/drain and junctionless configuration without dedicated source/drains.

- The whole simulation is done using classical drift-diffusion model. A more realistic scenario could be found with quantum effects beyond 20 nm NW thicknesses and energy balance models. However, QM effect is not expected to affect sub-threshold slope and DIBL significantly but it might make threshold voltage more negative due to quantum confinement associated effective oxide thickness increase beyond 20 nm nanowire thicknesses.

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APPENDIX A: Transfer Characteristics

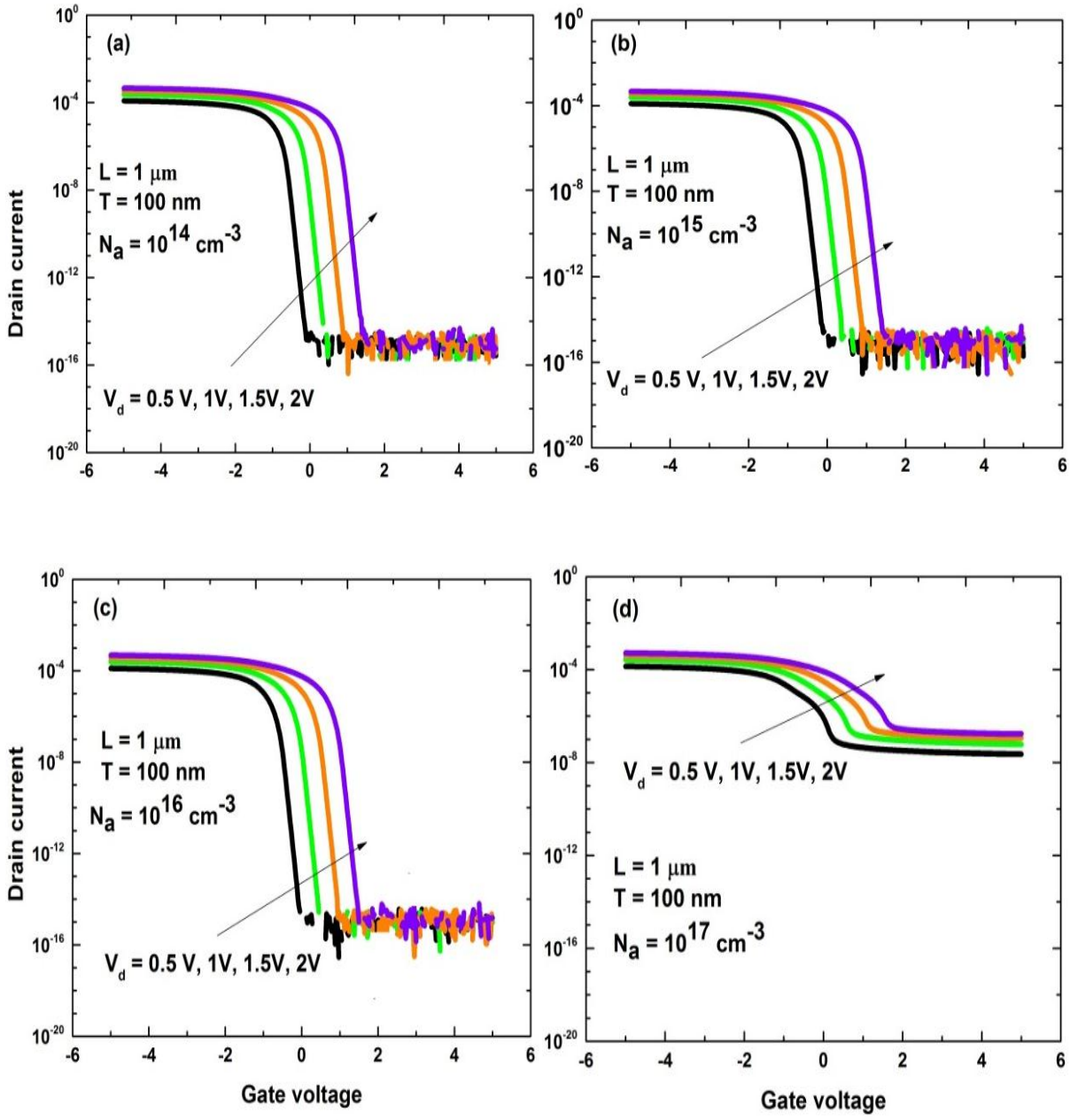

Figure A.1: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 100nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm. (**Continued to next page**)

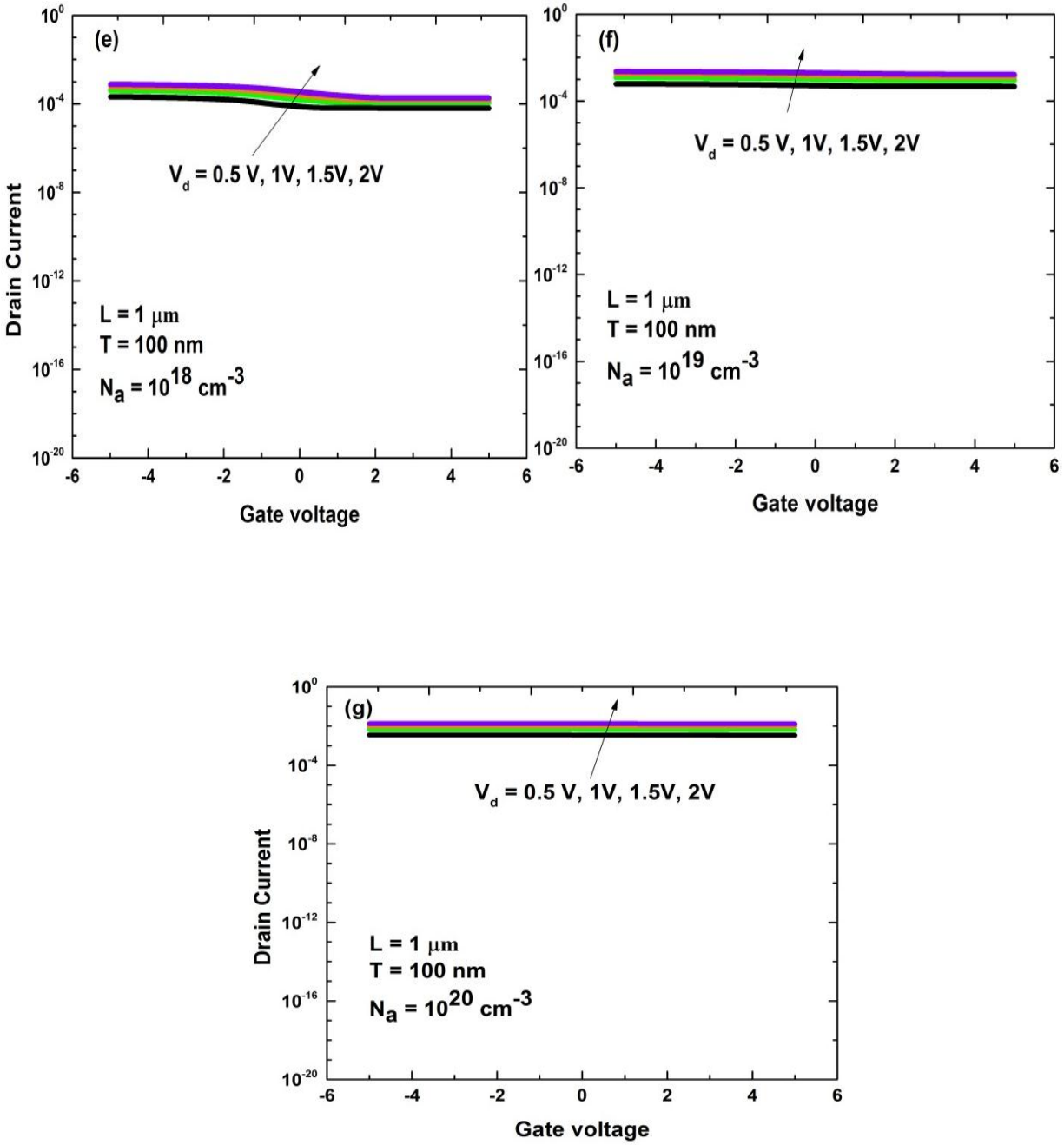

Figure A.1 **(continued)**: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 100nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm.

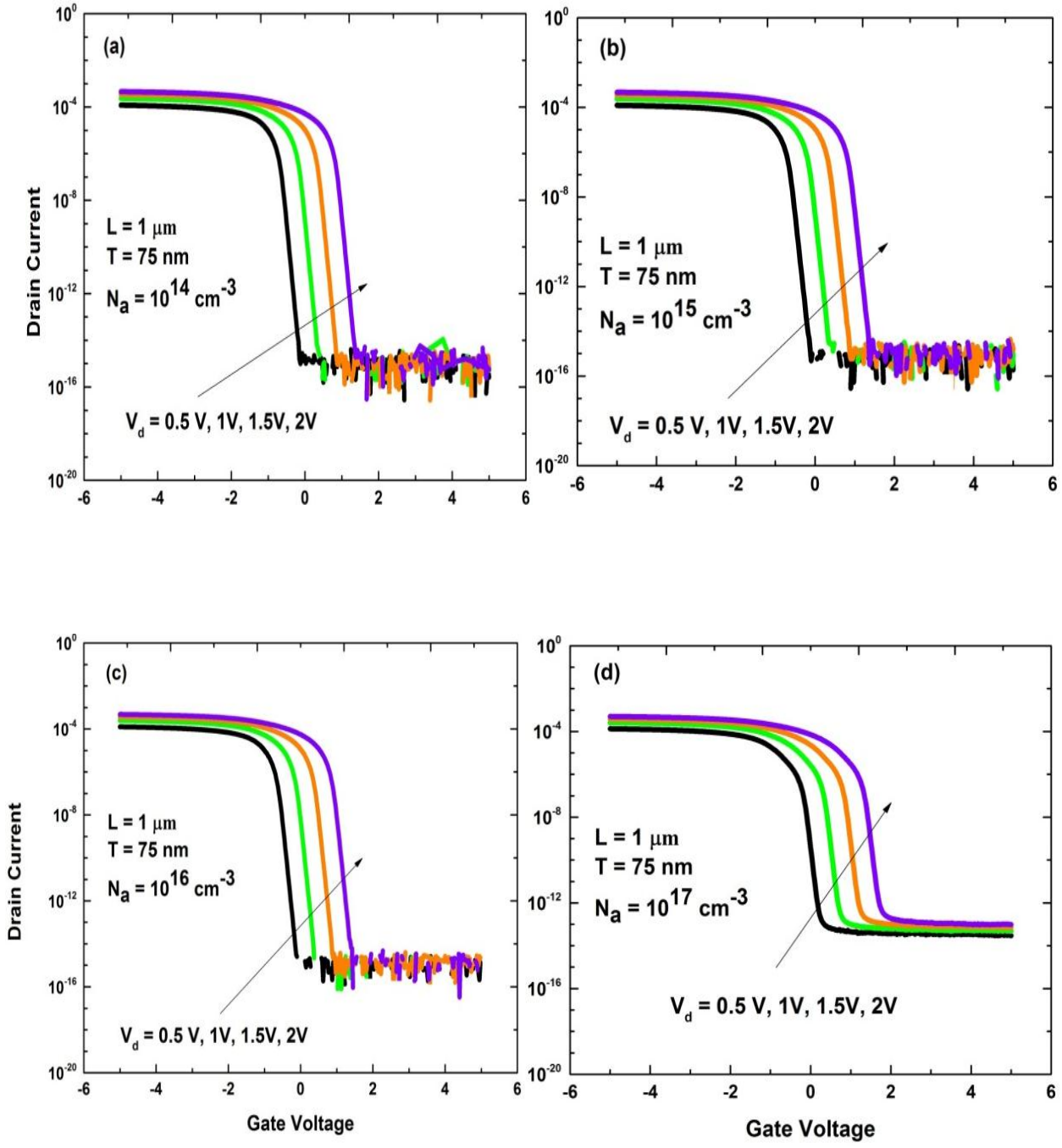

Figure A.2: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 75nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm. (**Continued to next page**)

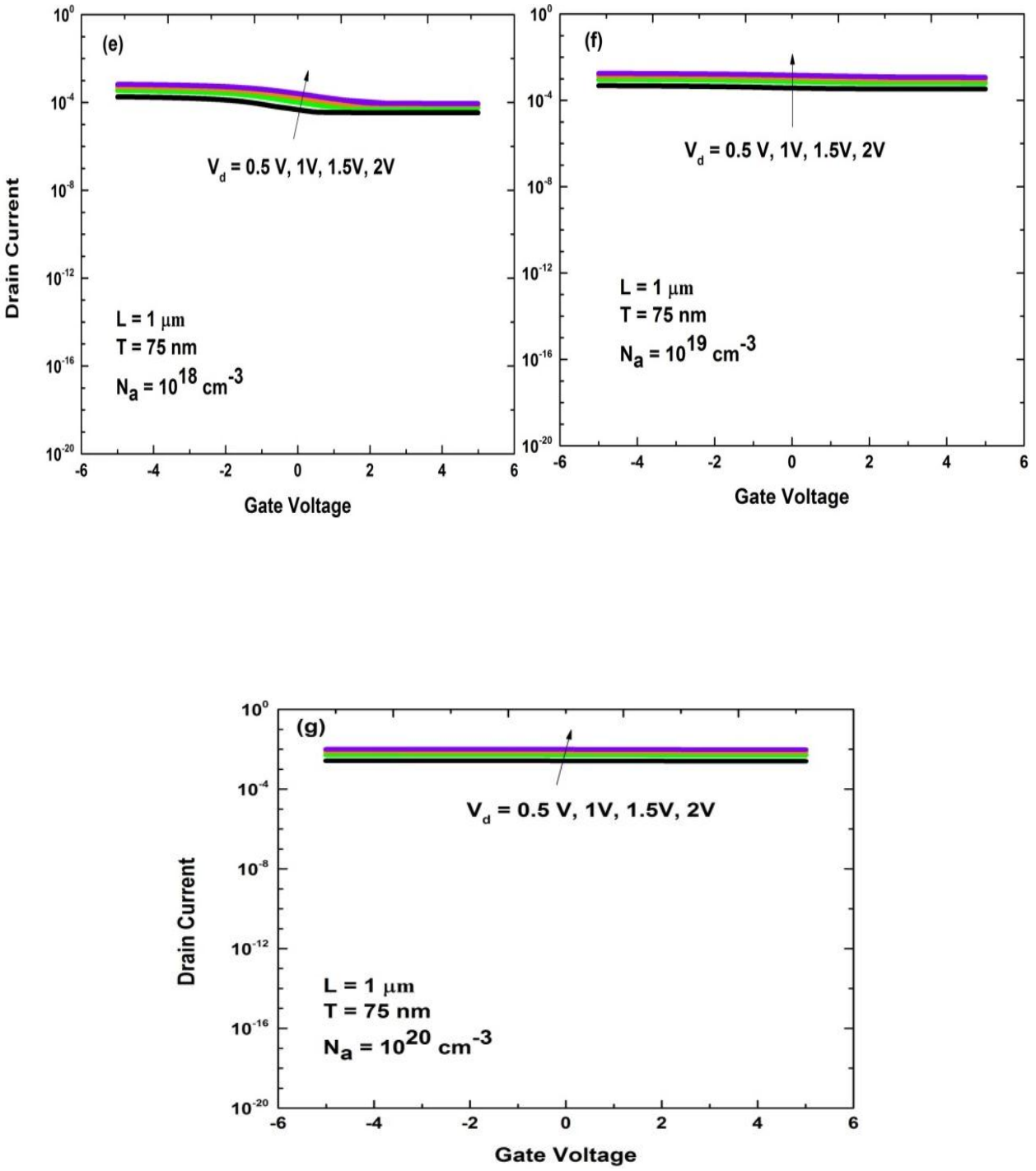

Figure A.2 **(continued)**: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 75nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm

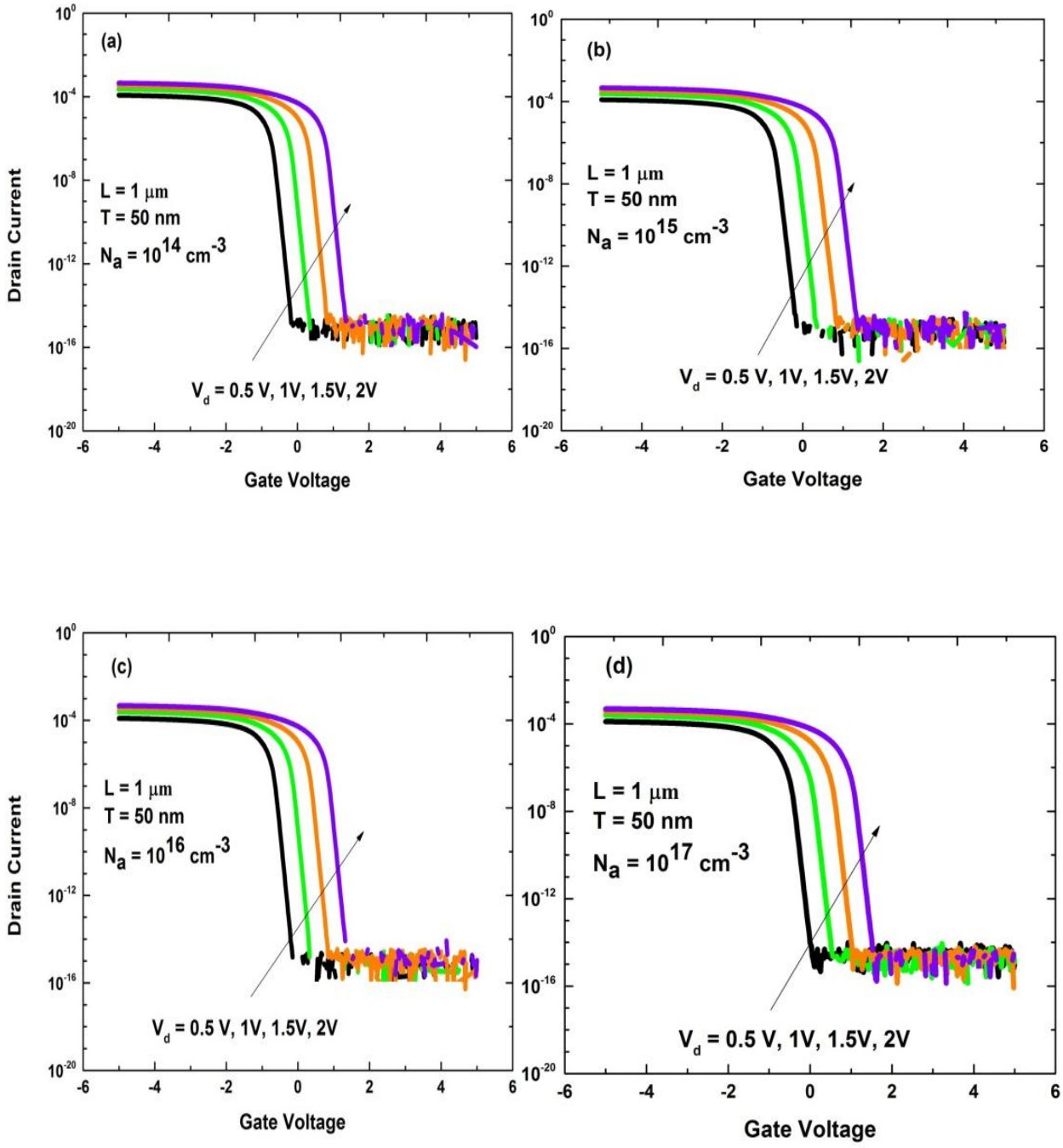

Figure A.3: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 50nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm. (**Continued to next page**)

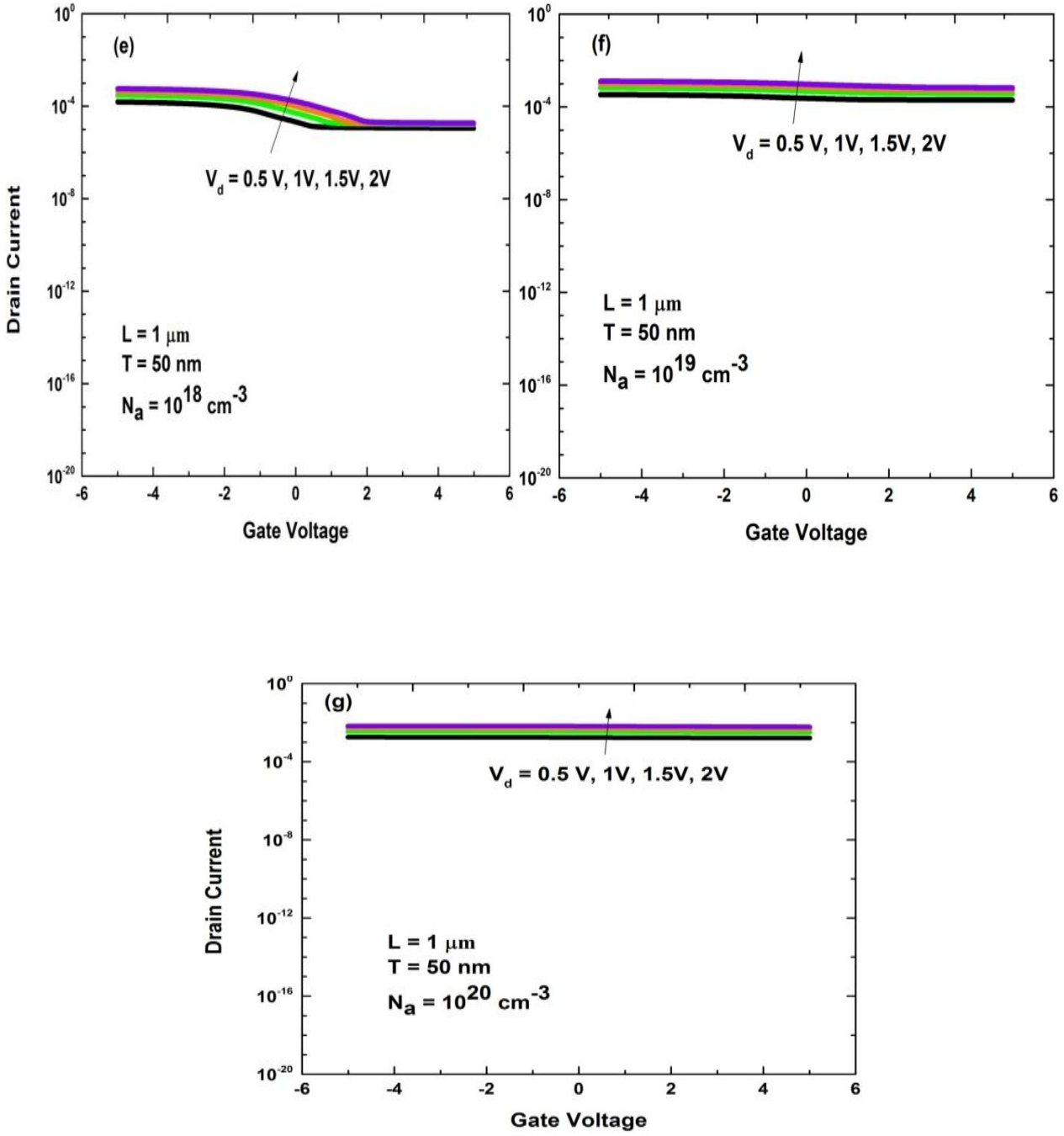

Figure A.3 **(continued)**: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 50nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm

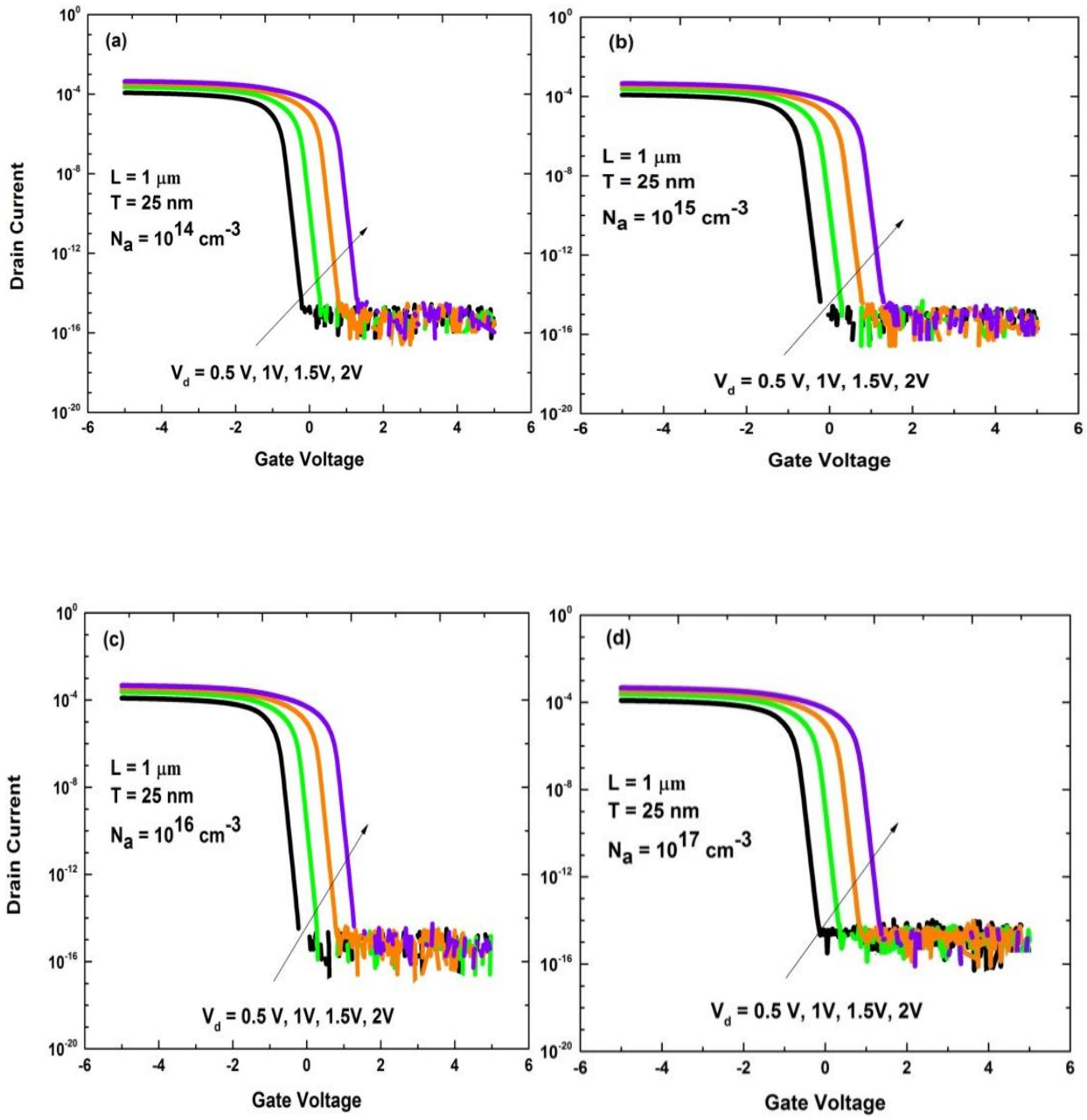

Figure A.4: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 25nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm. (**Continued to next page**)

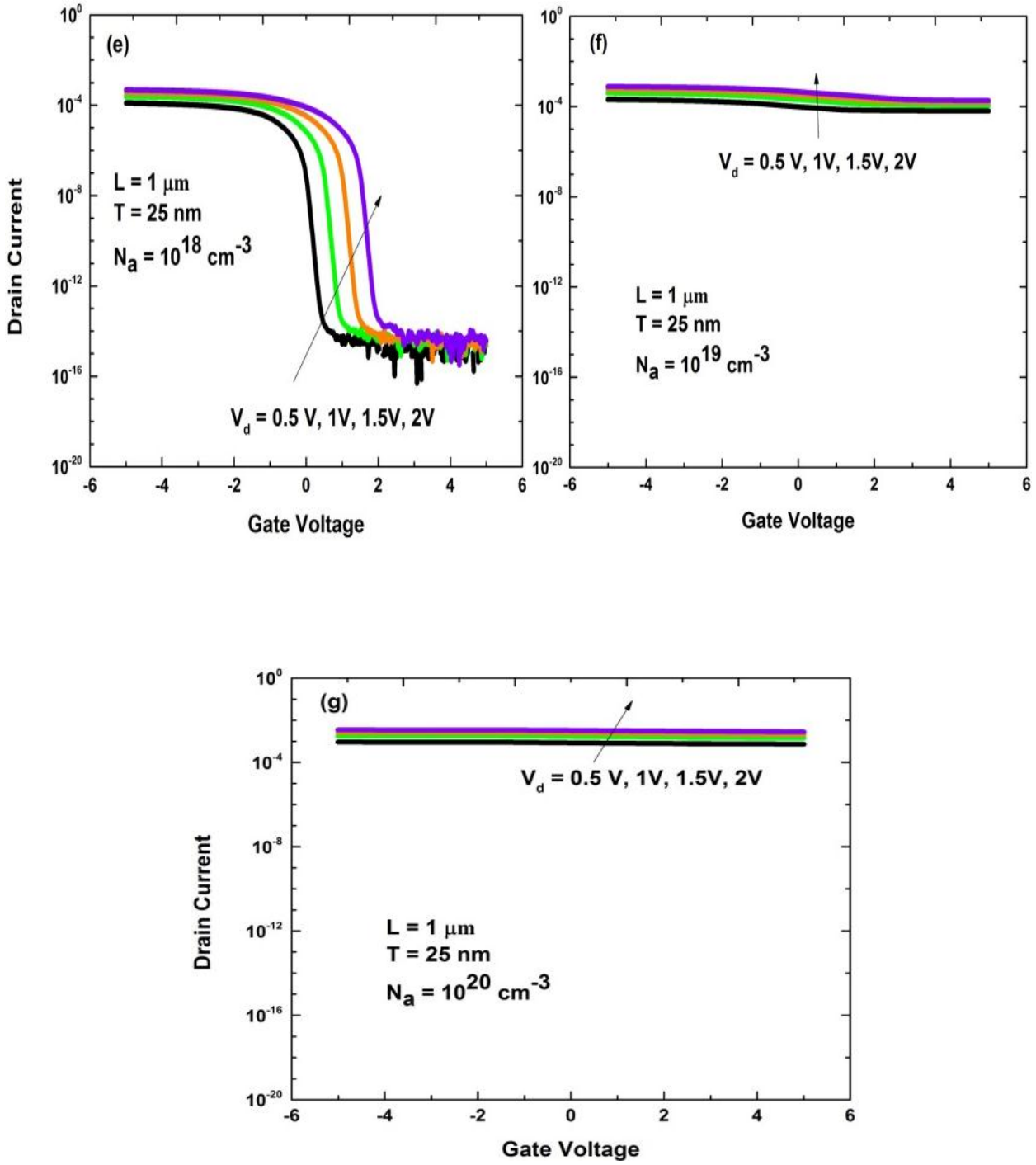

Figure A.4 **(continued)**: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 25nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm

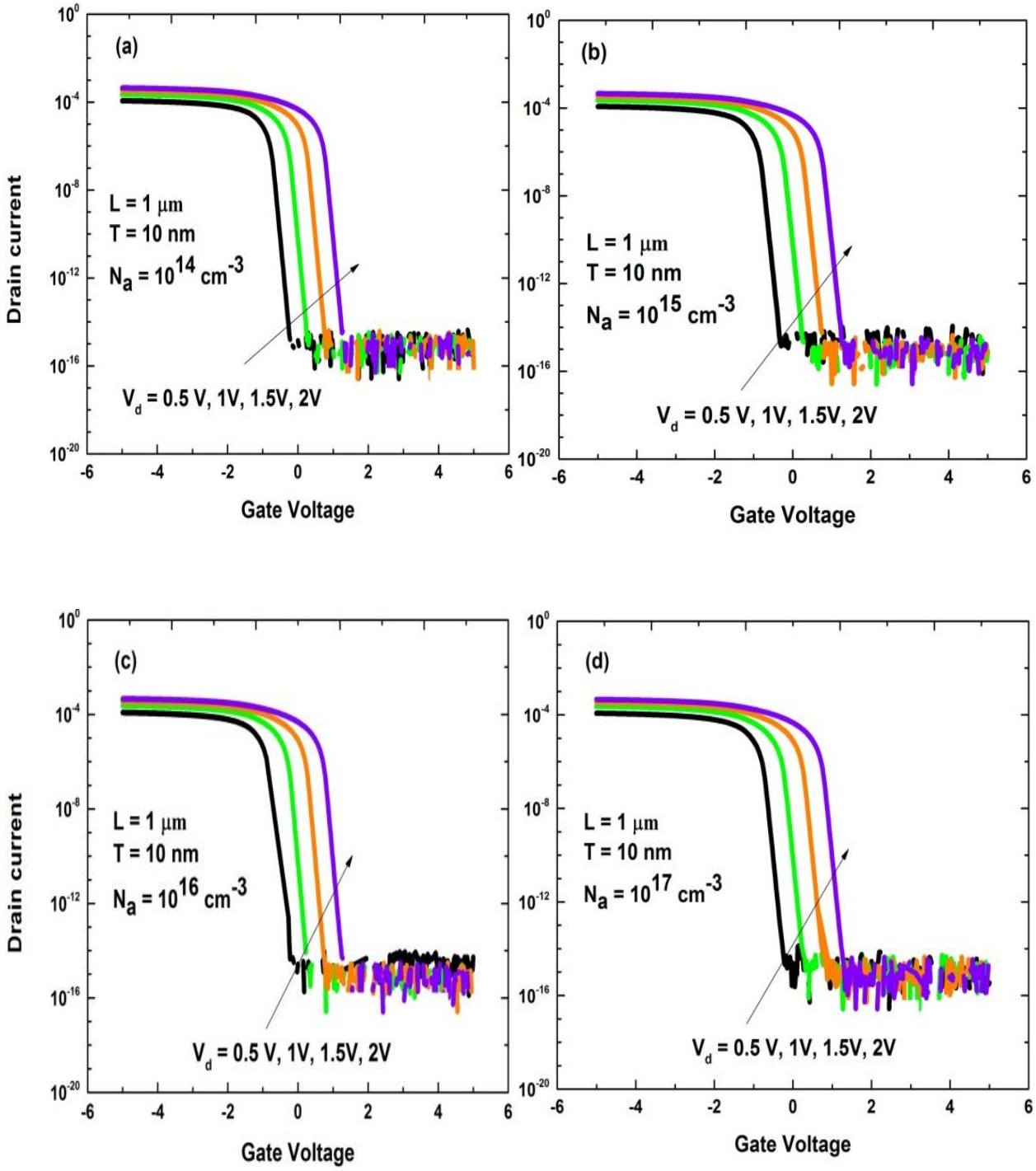

Figure A.5: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 10nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm. (**Continued to next page**)

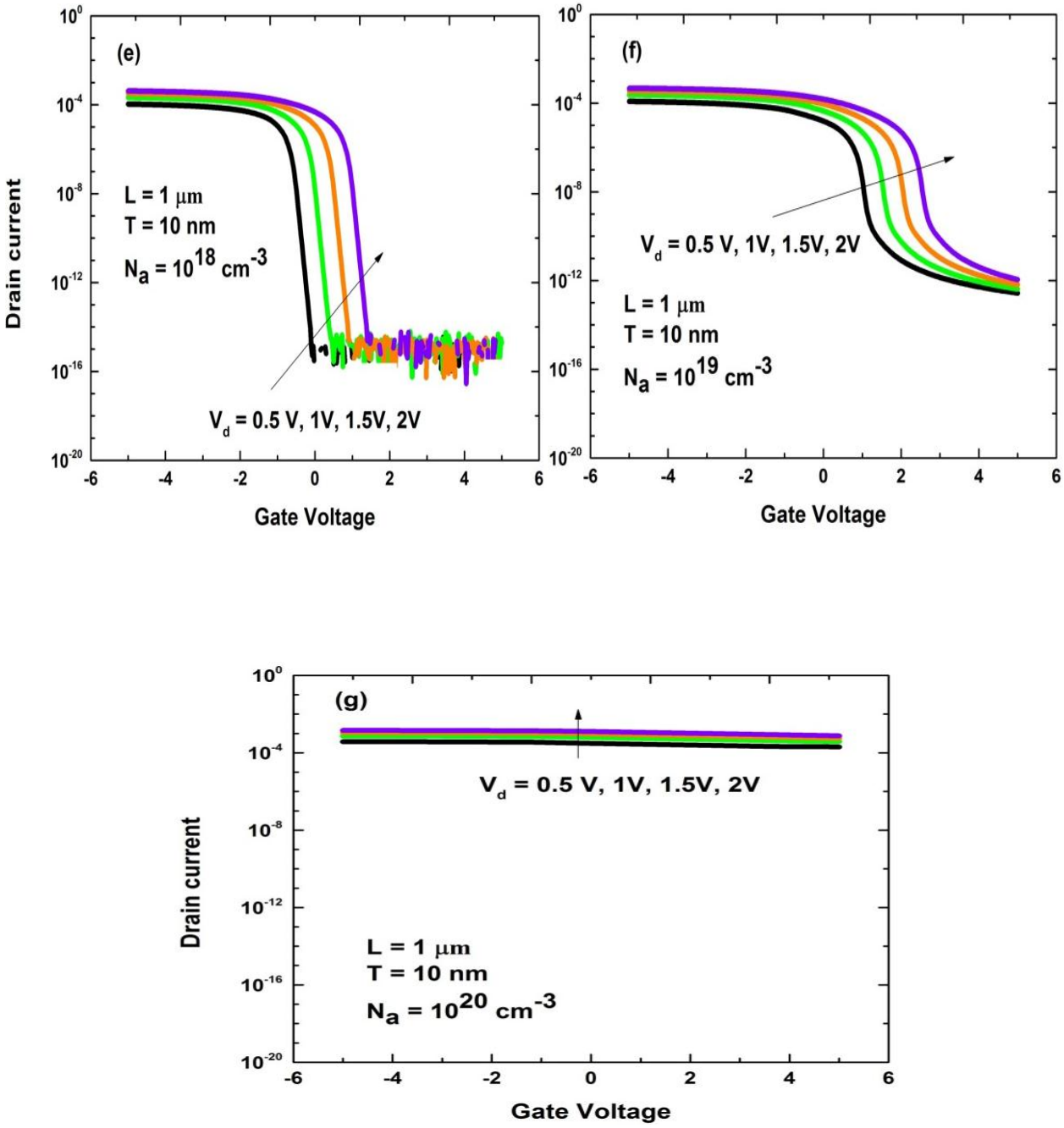

Figure A.5 **(continued)**: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 10nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm

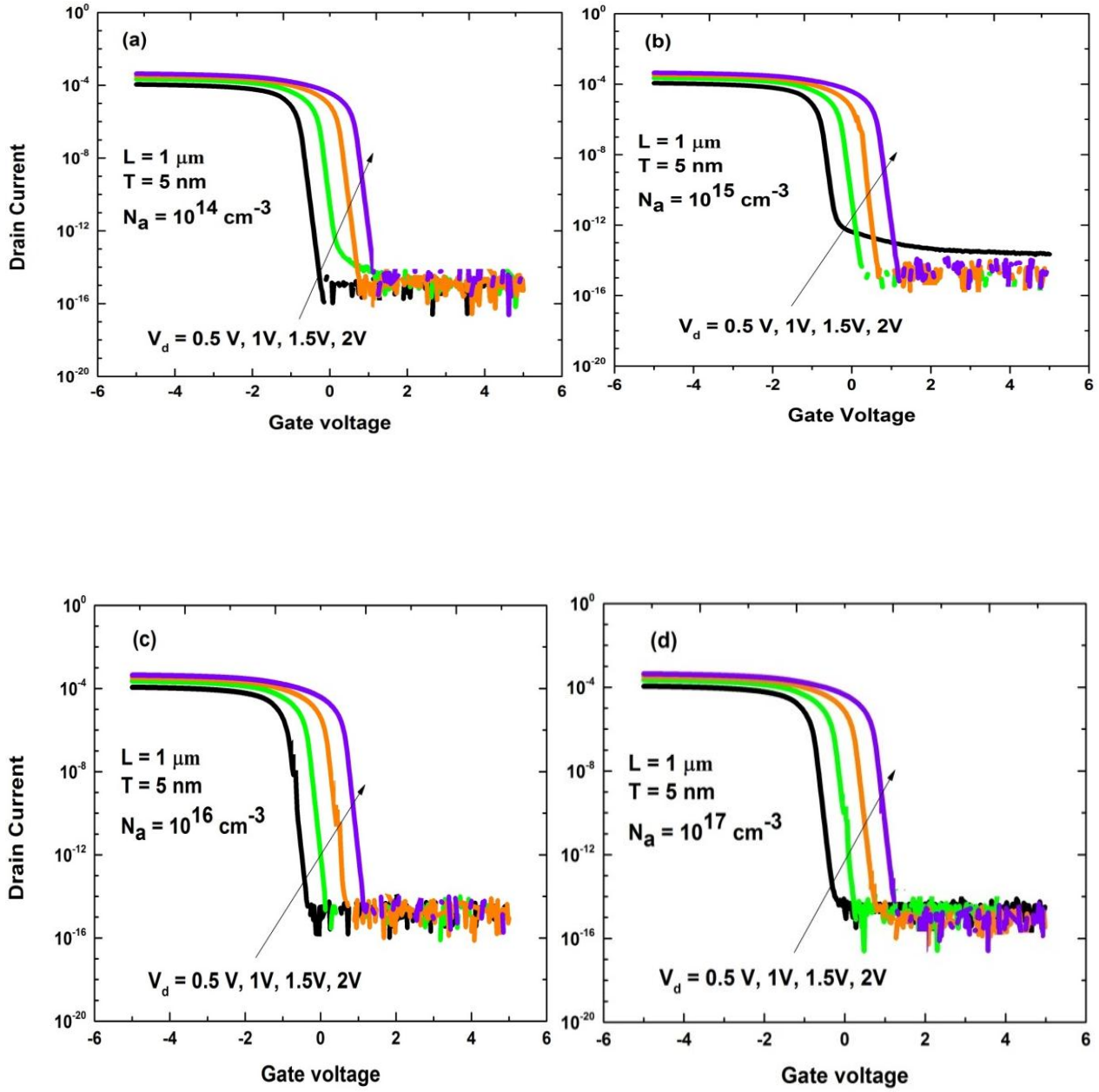

Figure A.6: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 5nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm. (**Continued to next page**)

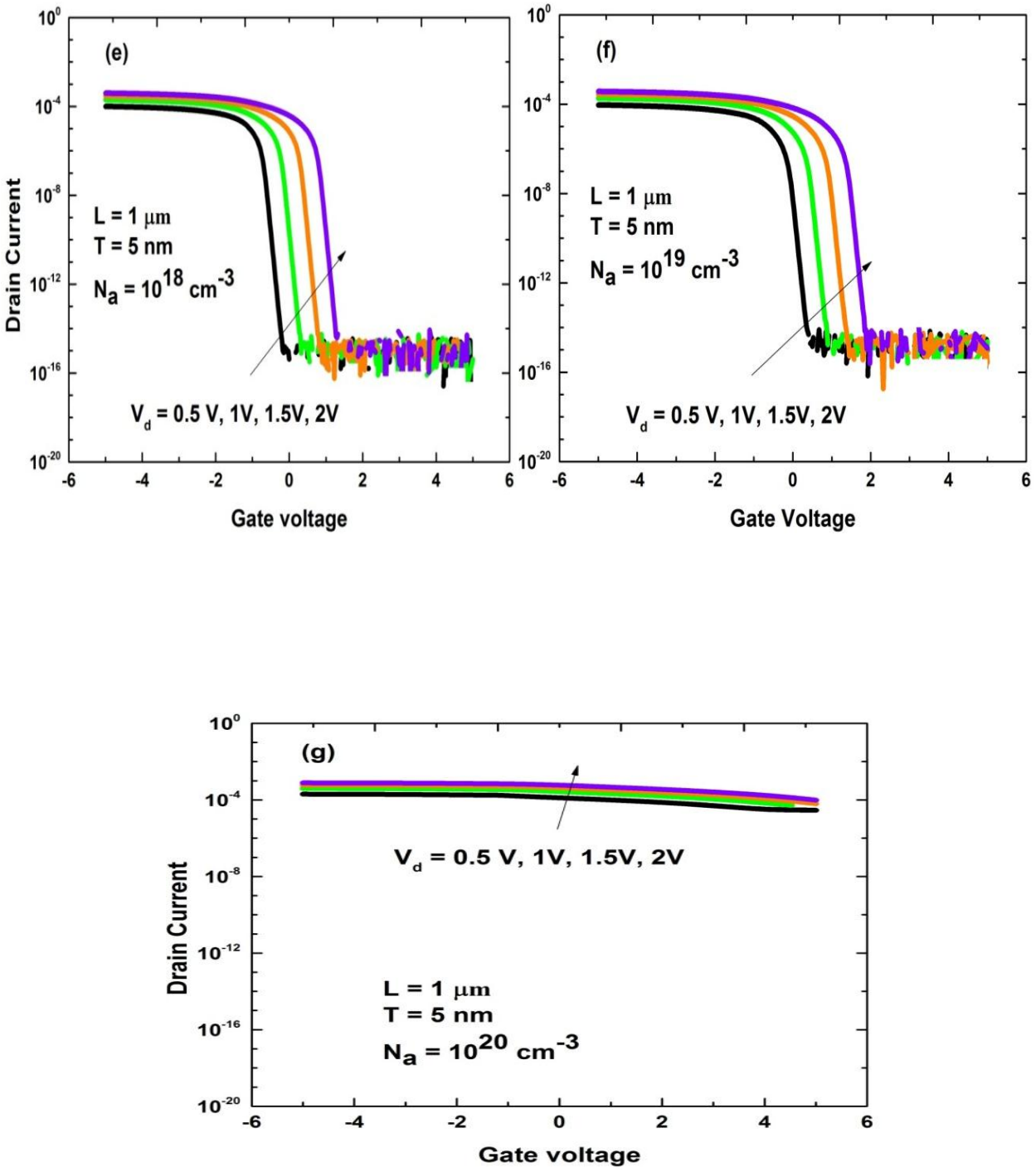

Figure A.6 **(continued)**: Transfer characteristics (I_D vs V_G) of accumulation mode SI-NW transistors with NW thickness of 5nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vs V_G curves for different drain voltages, i.e. 0.5 V, 1 V, 1.5 V and 2 V. NWs have channel length of 1μm

APPENDIX B: Output Characteristics

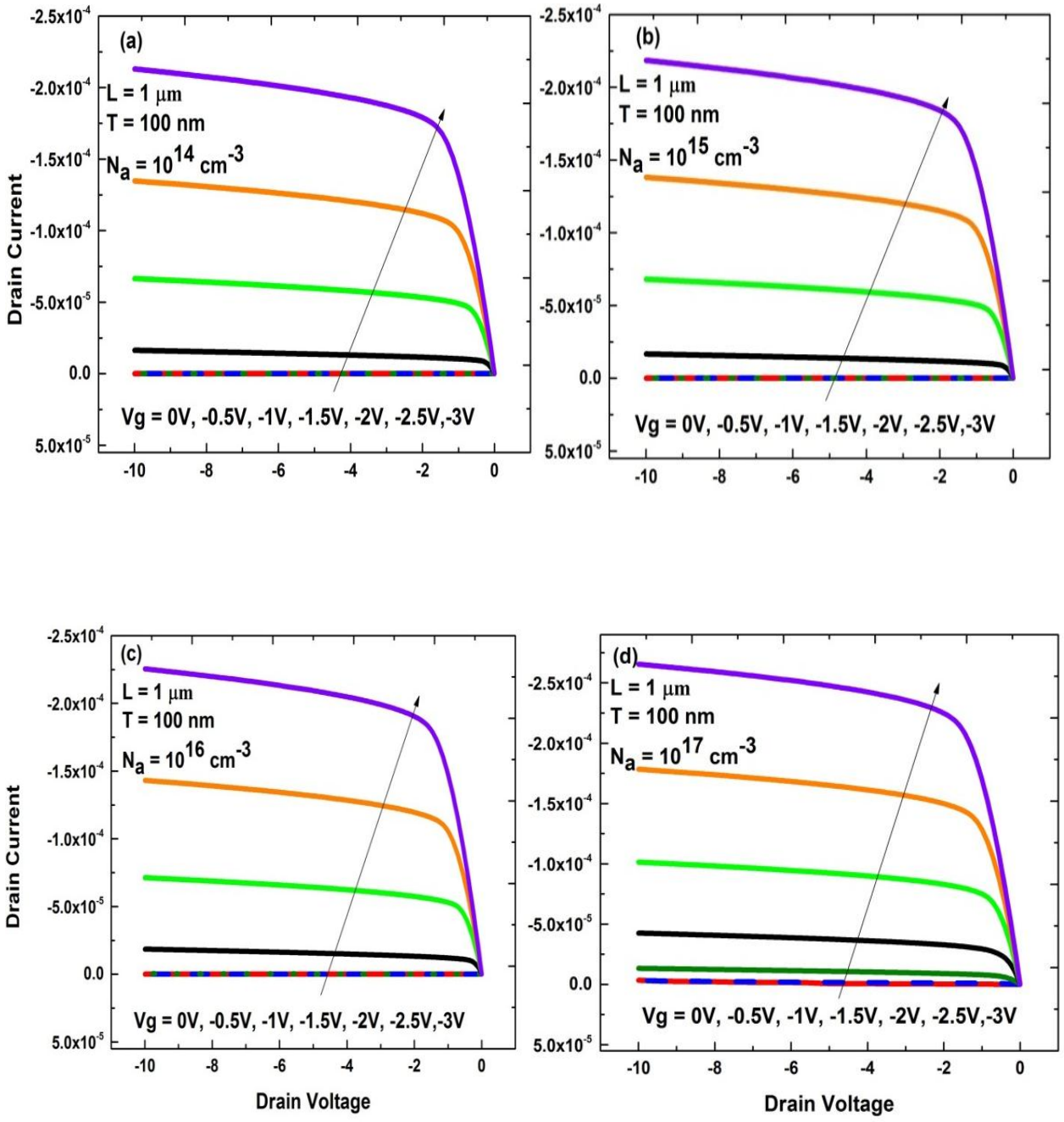

Figure B.1 : Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 100 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm. (**Continued to next page**)

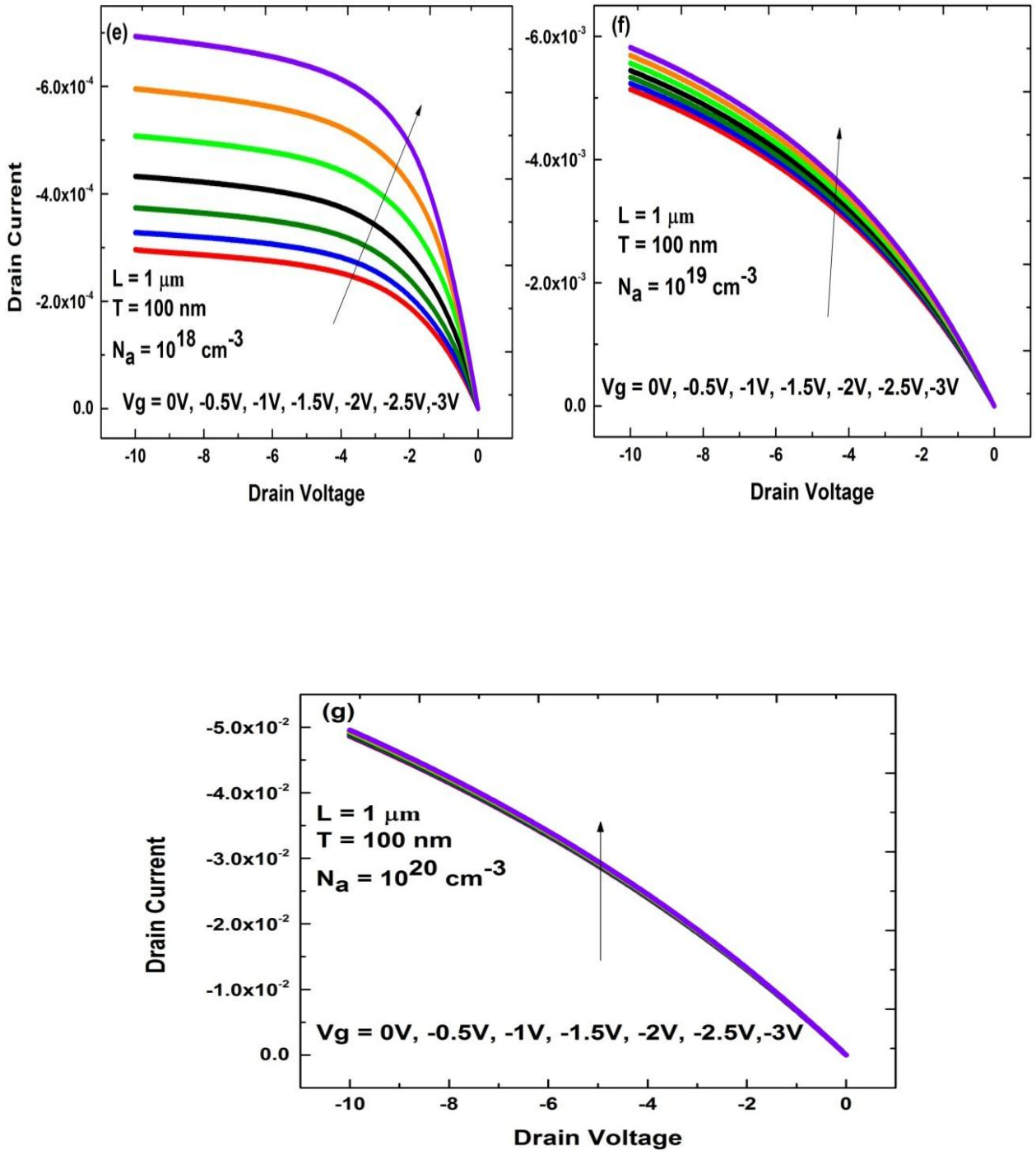

Figure B.1 **(continued)**: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 100 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm.

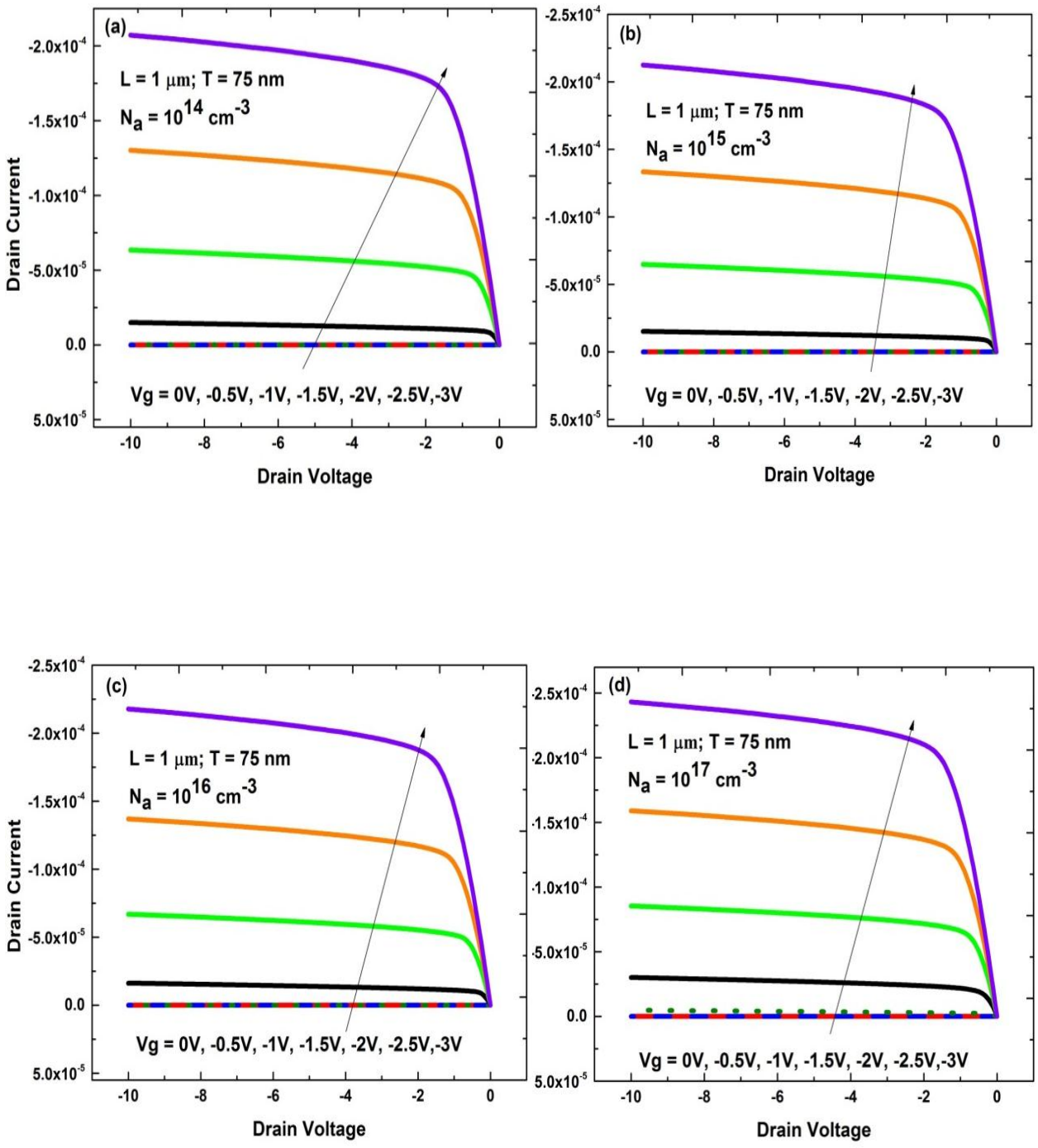

Figure B.2 : Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 75 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm. (**Continued to next page**)

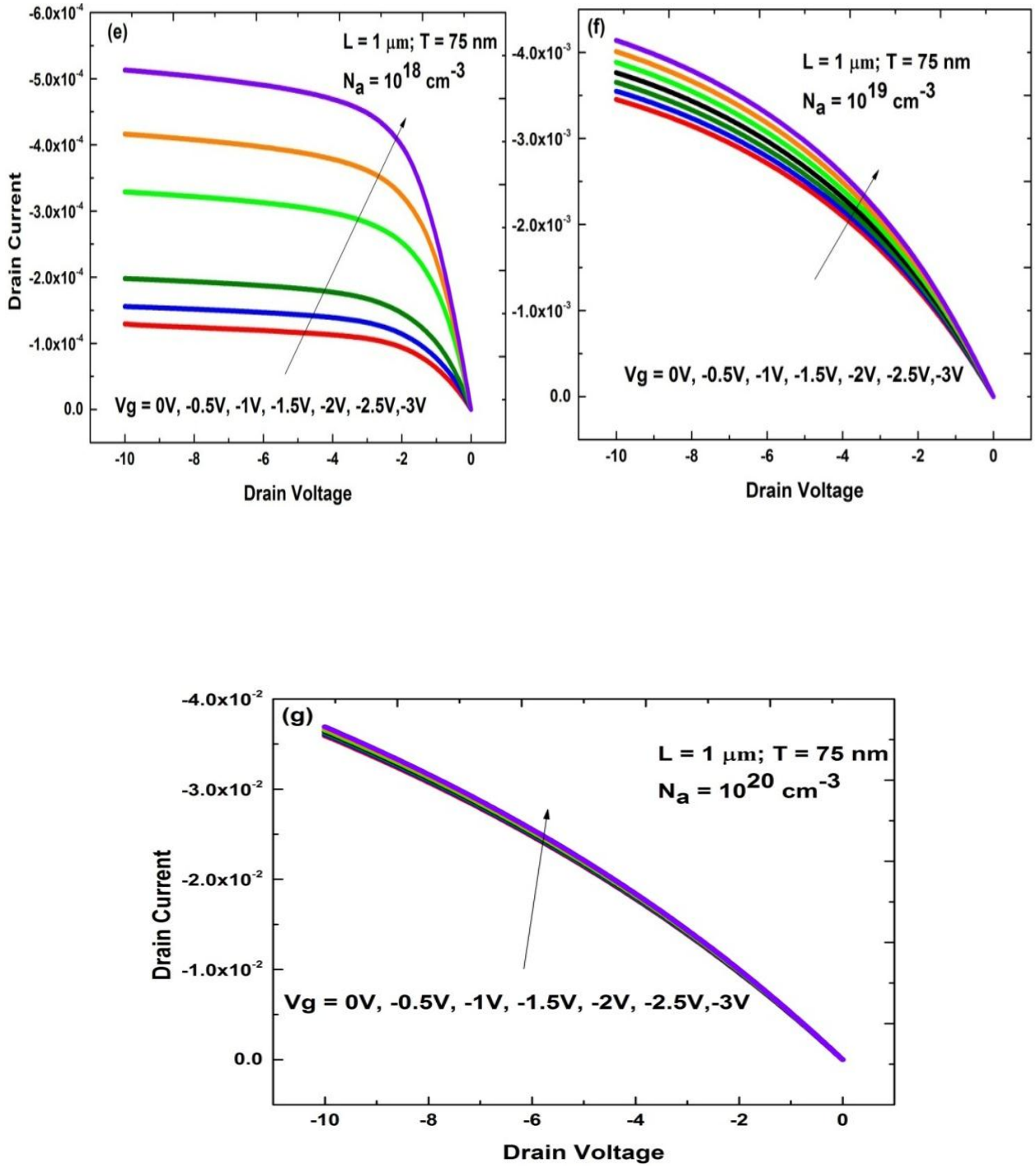

Figure B.2 **(continued)**: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 75 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm.

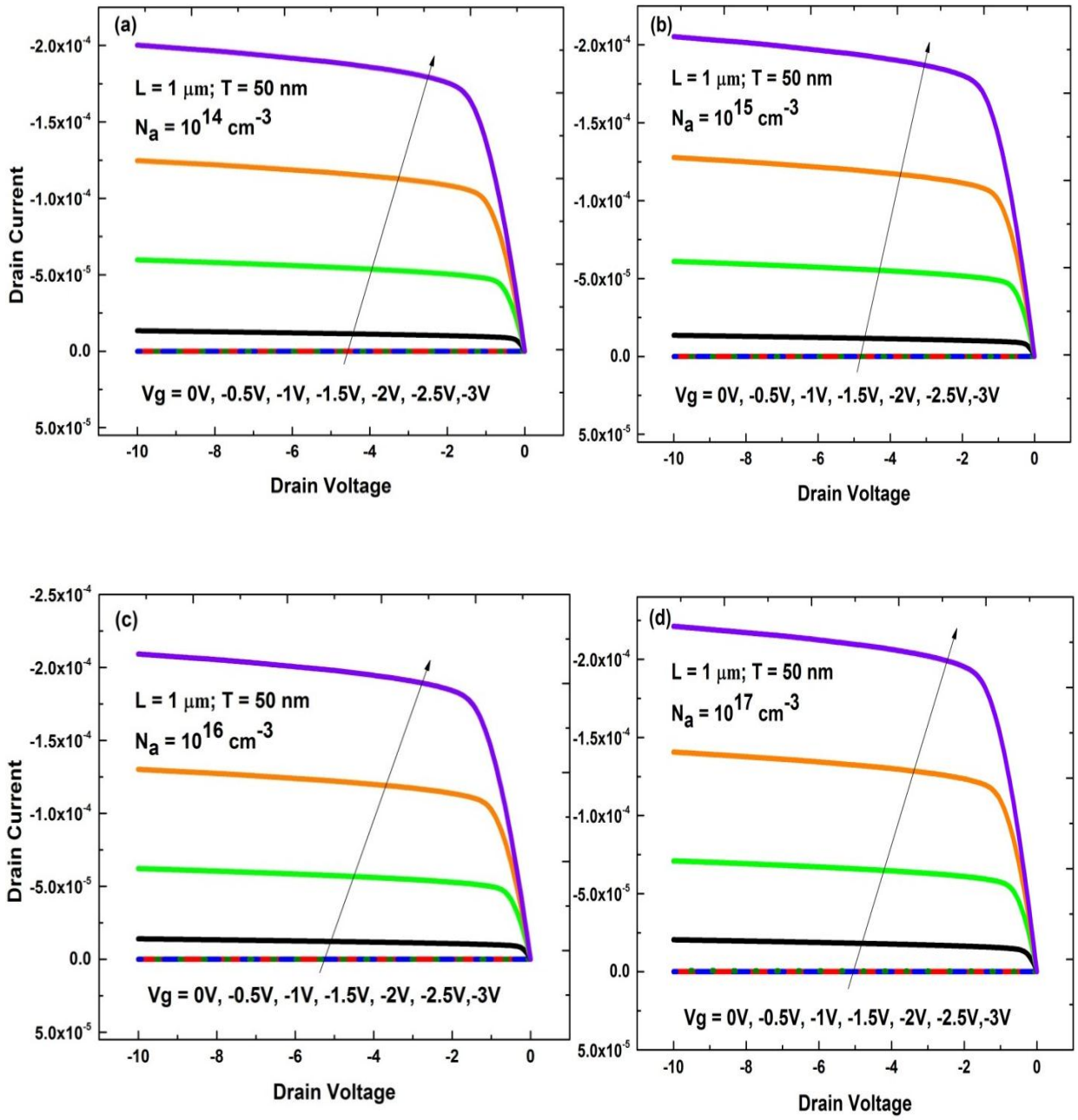

Figure B.3: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 50 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm. (**Continued to next page**)

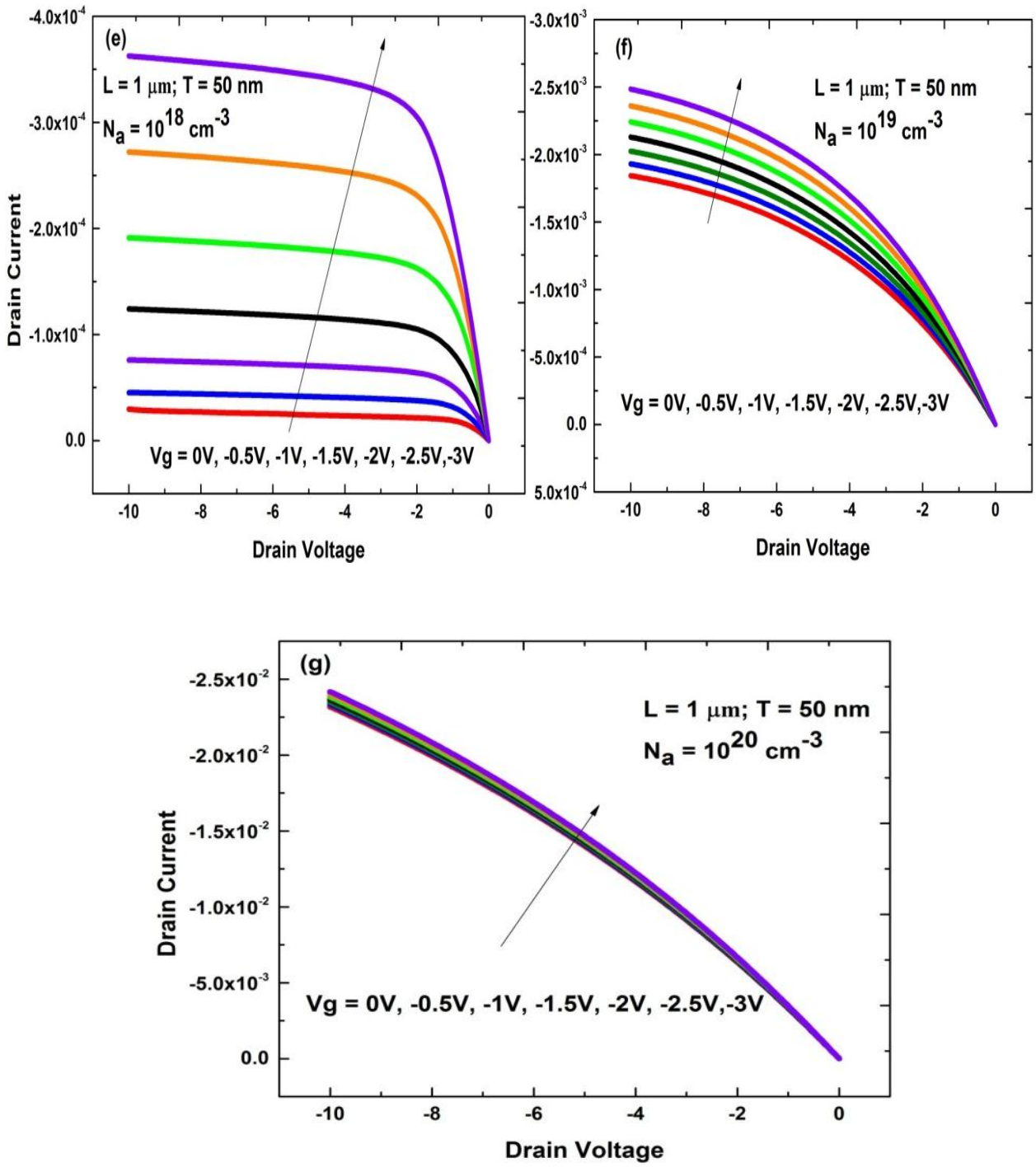

Figure B.3 **(continued)**: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 50 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm.

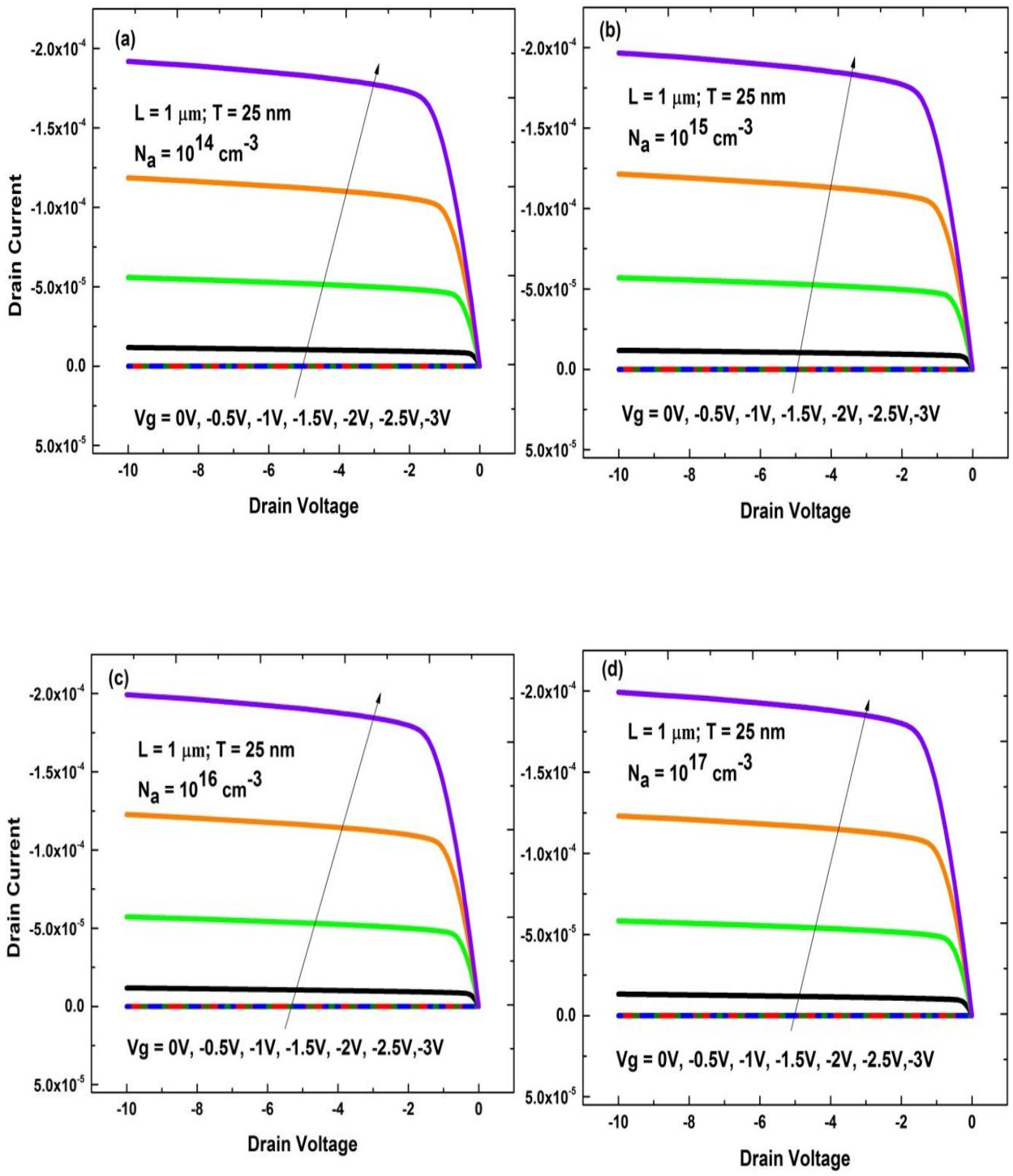

Figure B.4 : Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 25 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm. (**Continued to next page**)

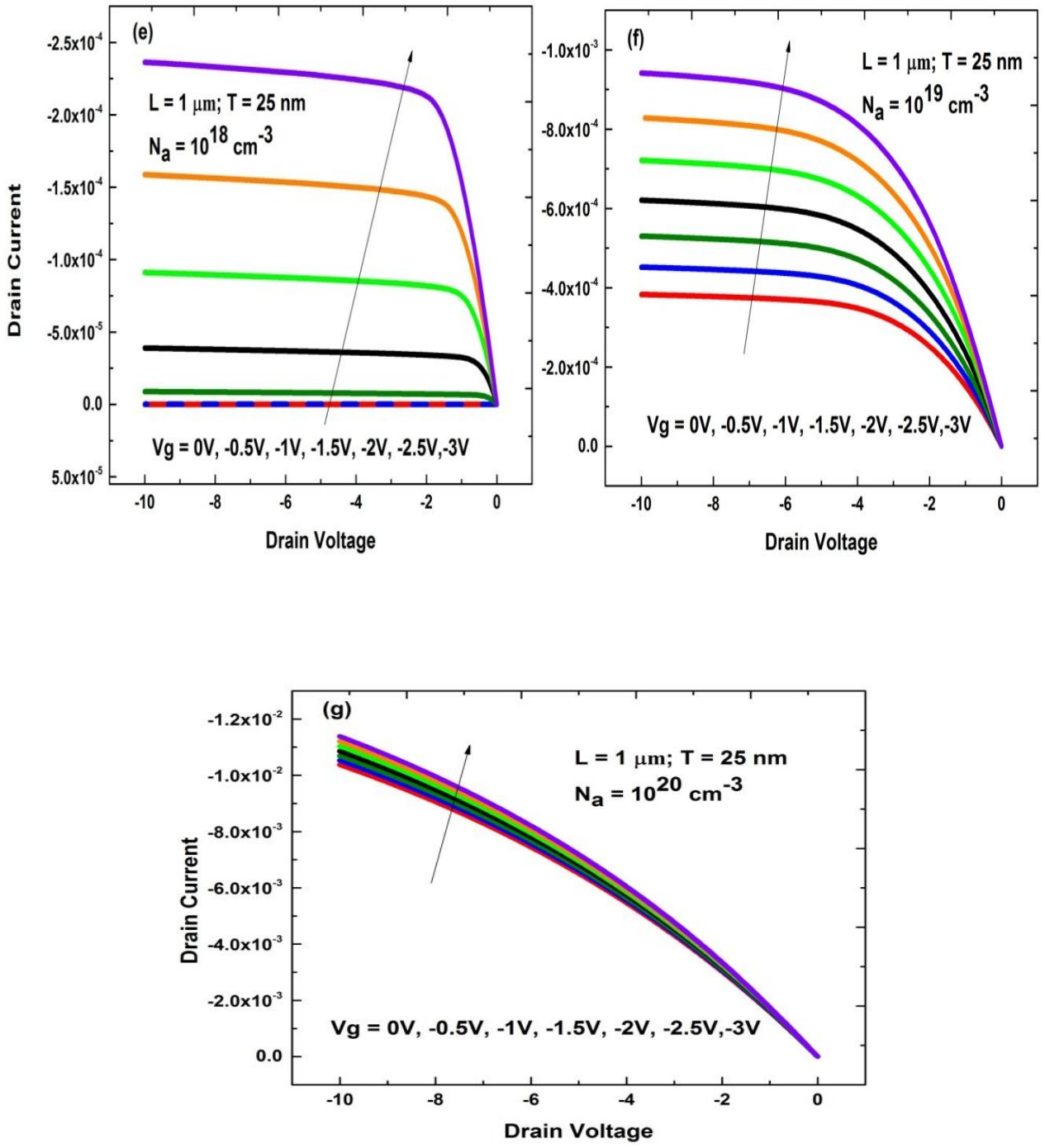

Figure B.4 **(continued)**: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 25 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm.

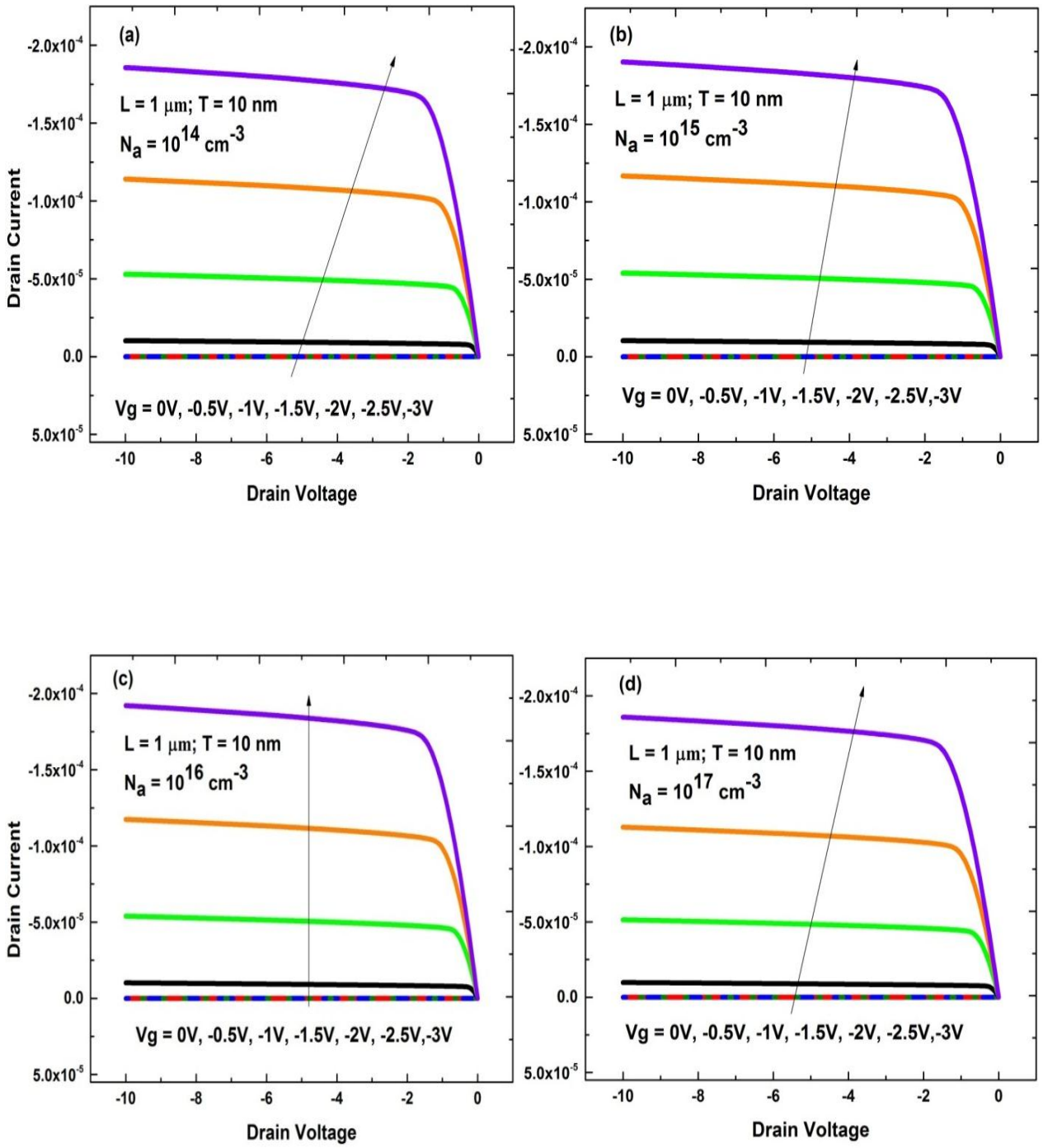

Figure B.5: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 10 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm. (**Continued to next page**)

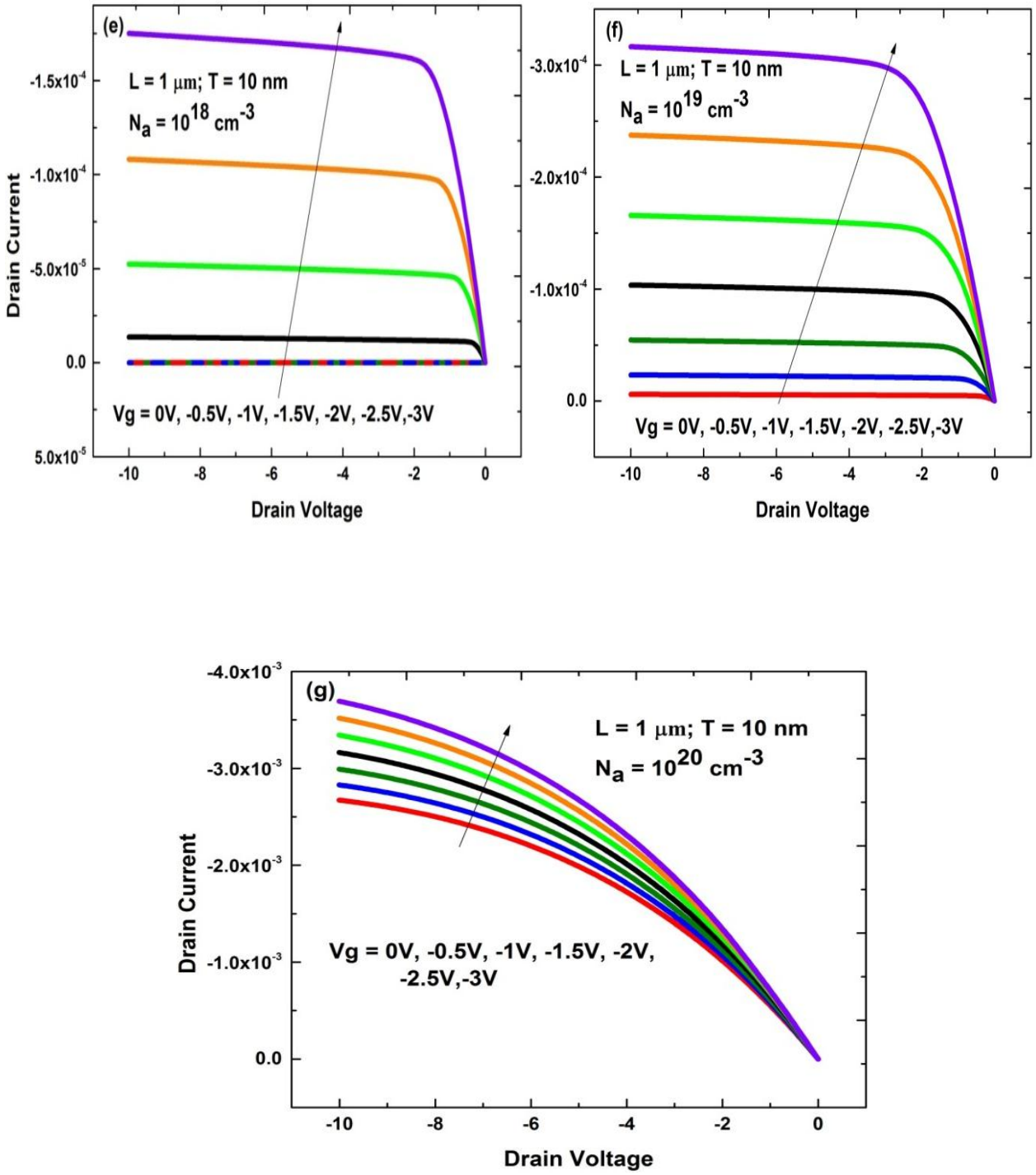

Figure B.5 **(continued)**: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 10 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm.

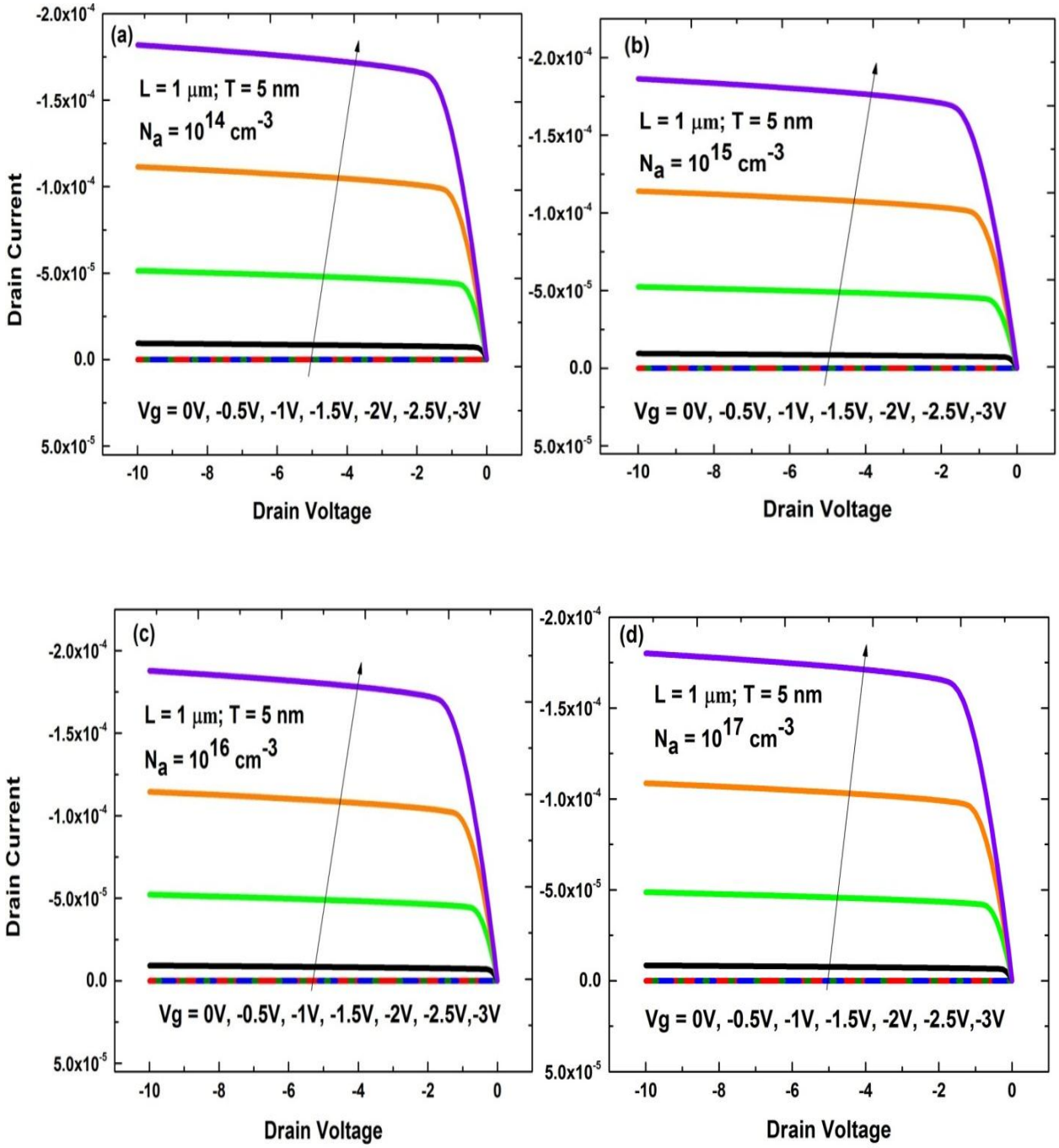

Figure B.6: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 5 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm. (**Continued to next page**)

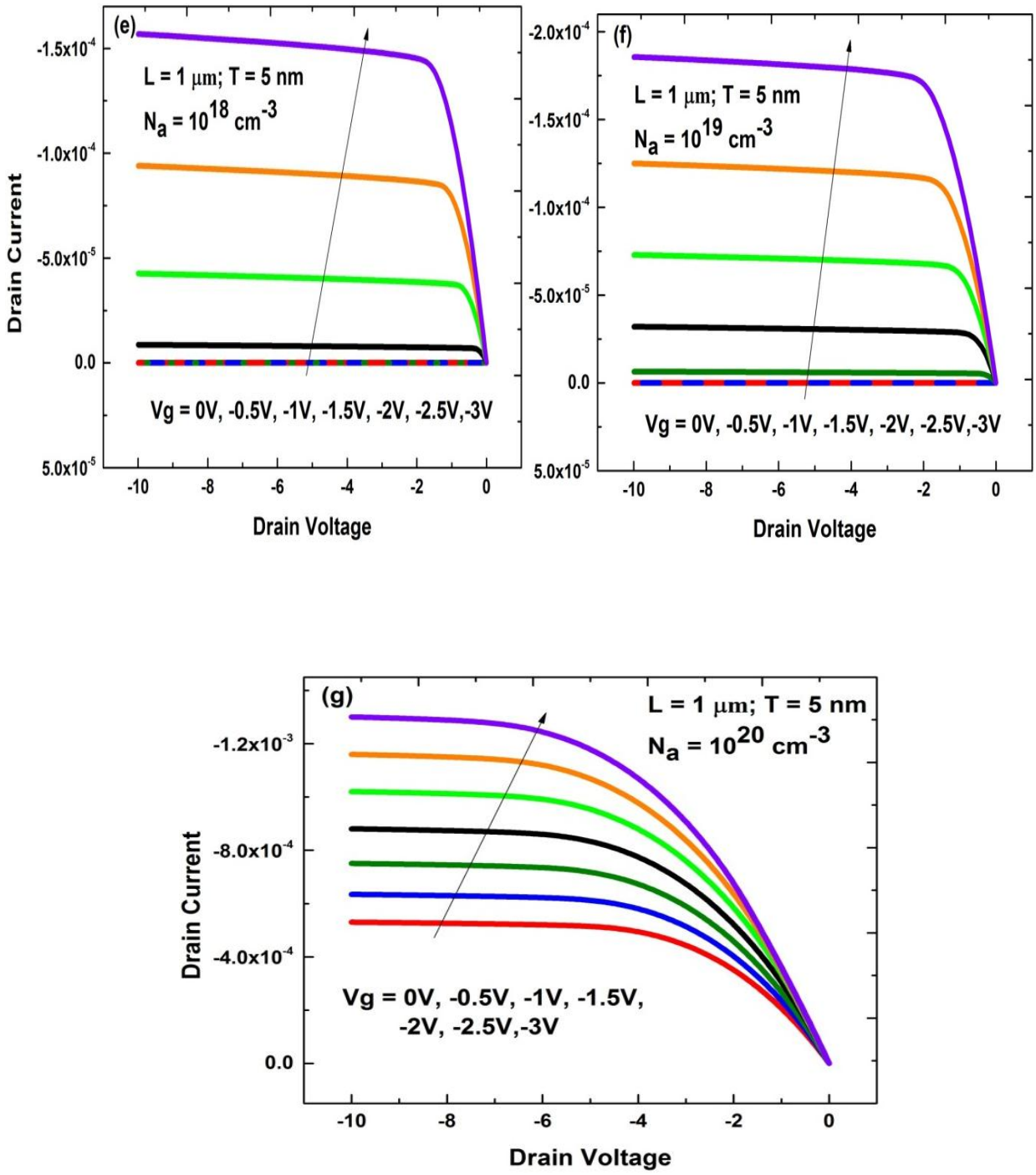

Figure B.6 **(continued)**: Simulated output characteristics (I_D vs V_D) of accumulation mode Si-NW transistors with NW thickness of 5 nm and doping concentrations of a) 10^{14} cm^{-3}, b) 10^{15} cm^{-3}, c) 10^{16} cm^{-3}, d) 10^{17} cm^{-3}, e) 10^{18} cm^{-3}, f) 10^{19} cm^{-3}, g) 10^{20} cm^{-3}. Different line colors represent I_D vsV_d curves for different gate voltages, i.e. 0 V, -0.5 V, -1 V, -1.5 V, -2 V, -2.5 V and -3 V. NWs have channel length of 1μm.

APPENDIX C: Data Tables

Table C.1: Data table of accumulation mode Si-NW transistors with NW thickness of 100nm.

Channel thickness	Doping concentration (cm^{-3})	Drain Voltage (v)	Subthreshold Slope(mv/dec)	Threshold voltage(v)	DIBL(mv/v)	Drive current (A/μm)
100nm	10^{14}	0.5V	66.4696	-0.75	982	5.97e-5
		1V	66.7359	-0.225		
		1.5V	66.8154	0.28		
		2V	70.0670	0.8		
	10^{15}	0.5V	66.4696	-0.75	982	6.11e-5
		1V	66.7359	-0.225		
		1.5V	66.8154	0.28		
		2V	70.0670	0.8		
	10^{16}	0.5V	67.9219	-0.75	982	6.42e-5
		1V	66.79	-0.175		
		1.5V	66.9924	0.33		

		2V	67.9728	0.85		
	10^{17}	0.5V	777.33	-0.025	1500	9.23e-5
		1V	846.83	0.5		
		1.5V	854.8754	1		
		2V	845.5287	1.52		
	10^{18}	0.5V	5.9426e+003	Not measureable	3.9000e+003	0.000464
		1V	6.0962e+003	Not measureable		
		1.5V	6.1578e+003	Not measureable		
		2V	6.3397e+003	Not measureable		
	10^{19}	0.5V	Not measurable	Not measureable	Not measurable	0.00392
		1V	Not measurable	Not measureable		
		1.5V	Not measurable	Not measureable		
		2V	Not measurable	Not measureable		
	10^{20}	0.5V	Not measurable	Not measurable	Not measurable	0.0295
		1V	Not measurable	Not measureable		
		1.5V	Not measurable	Not measureable		
		2V	Not measurable	Not measureable		

Table C.2: Data table of accumulation mode Si-NW transistors with NW thickness of 75nm.

Channel thickness	Doping concentration (cm^{-3})	Drain Voltage (v)	Subthreshold Slope(mv/dec)	Threshold voltage(v)	DIBL(mv/v)	Drive current (A/μm)
75nm	10^{14}	0.5V	64.5	-0.75	1008	5.76e-5
		1V	64	-0.225		
		1.5V	64	0.275		
		2V	64.6	0.75		
	10^{15}	0.5V	64.5	-0.75	1008	5.89e-5
		1V	64	-0.225		
		1.5V	64	0.275		
		2V	64.6	0.75		
	10^{16}	0.5V	64.5	-0.72	1008	6.09e-5
		1V	64.8	-0.198		
		1.5V	65.1	0.299		
		2V	67.9	0.81		

	10^{17}	0.5V	69.3	-0.368	1058	7.85e-5
		1V	72	0.135		
		1.5V	71.7	0.652		
		2V	76.2	1.17		
	10^{18}	0.5V	4080	Not measurable	2713	0.000306
		1V	4130	Not measurable		
		1.5V	4180	Not measurable		
		2V	4250	Not measurable		
	10^{19}	0.5V	Not measurable	Not measurable	Not measurable	0.00276
		1V	Not measurable	Not measurable		
		1.5V	Not measurable	Not measurable		
		2V	Not measurable	Not measurable		
	10^{20}	0.5V	Not measurable	Not measurable	Not measurable	0.0219
		1V	Not measurable	Not measurable		
		1.5V	Not measurable	Not measurable		
		2V	Not measurable	Not measurable		

Table C.3: Data table of accumulation mode Si-NW transistors with NW thickness of 50nm.

Channel thickness	Doping concentration (cm^{-3})	Drain Voltage (v)	Subthreshold Slope (mv/dec)	Threshold voltage(v)	DIBL (mv/v)	Drive current (A/μm)
50nm	10^{14}	0.5V	64.0965	-0.75	982.2	5.49e-5
		1V	63.8929	-0.246		
		1.5V	63.2561	0.258		
		2V	64.3636	0.762		
	10^{15}	0.5V	64.0965	-0.75	982.2	5.61e-5
		1V	63.8929	-0.246		
		1.5V	63.2561	0.258		
		2V	64.3636	0.762		
	10^{16}	0.5V	64.0965	-0.75	982.2	5.73e-5
		1V	63.8929	-0.246		
		1.5V	63.2561	0.258		
		2V	64.3636	0.762		

	10^{17}	0.5V	65.0554	-0.586	1008	6.59e-5
		1V	64.7202	-0.082		
		1.5V	63.2635	0.409		
		2V	65.3222	0.926		
	10^{18}	0.5V	2.3966e+003	Not measureable	1889.2	0.00018
		1V	2.3779e+003	Not measureable		
		1.5V	2.3140e+003	Not measureable		
		2V	476.9993	Not measureable		
	10^{19}	0.5V	1.6516e+004	Not measureable	Not measureable	0.00171
		1V	1.7553e+004	Not measureable		
		1.5V	1.8561e+004	Not measureable		
		2V	1.9208e+004	Not measureable		
	10^{20}	0.5V	Not measureable	Not measureable	Not measureable	0.0141
		1V	Not measureable	Not measureable		
		1.5V	Not measureable	Not measureable		
		2V	Not measureable	Not measureable		

Table C.4: Data table of accumulation mode Si-NW transistors with NW thickness of 25nm.

Channel thickness	Doping concentration (cm^{-3})	Drain Voltage (v)	Subthreshold Slope (mv/dec)	Threshold voltage(v)	DIBL(mv/v)	Drive current (A/μm)
25nm	10^{14}	0.5V	61.8	-0.762	1000	5.19e-5
		1V	61.9	-0.258		
		1.5V	61	0.233		
		2V	61	0.749		
	10^{15}	0.5V	61.8	-0.762	1000	5.3e-5
		1V	61.9	-0.258		
		1.5V	61	0.233		
		2V	61	0.749		
	10^{16}	0.5V	61.8	-0.762	1000	5.34e-5
		1V	61.9	-0.258		
		1.5V	61	0.233		
		2V	61	0.749		

	10^{17}	0.5V	63.3	-0.732	1000	5.45e-5
		1V	64.4	-0.225		
		1.5V	64.7	0.279		
		2V	64.6	0.779		
	10^{18}	0.5V	66	-0.184	1000	8.65e-5
		1V	69.1	0.323		
		1.5V	65.7	0.824		
		2V	69.7	1.33		
	10^{19}	0.5V	8.00E+03	Not measureable	Not measureable	0.000673
		1V	8.01E+03	Not measureable		
		1.5V	8.20E+03	Not measureable		
		2V	8.06E+03	Not measureable		
	10^{20}	0.5V	Not measureable	Not measureable	Not measureable	0.00696
		1V	Not measureable	Not measureable		
		1.5V	Not measureable	Not measureable		
		2V	Not measureable	Not measureable		

Table C.5: Data table of accumulation mode Si-NW transistors with NW thickness of 10nm.

Channel thickness	Doping concentration (cm^{-3})	Drain Voltage (v)	Subthreshold Slope (mv/dec)	Threshold voltage(v)	DIBL(mv/v)	Drive current (A/μm)
10nm	10^{14}	0.5V	61.8	-0.785	1000	4.97e-5
		1V	62.3	-0.3		
		1.5V	61.1	0.2		
		2V	62.2	0.7		
	10^{15}	0.5V	61.8	-0.785	1000	5.07e-5
		1V	62.3	-0.3		
		1.5V	61.1	0.2		
		2V	62.2	0.7		
	10^{16}	0.5V	61.8	-0.785	1000	5.07e-5
		1V	62.3	-0.3		
		1.5V	61.1	0.2		
		2V	62.2	0.7		

	10^{17}	0.5V	61.8	-0.785	1000	4.83e-5
		1V	62.3	-0.3		
		1.5V	61.1	0.22		
		2V	62.2	0.73		
	10^{18}	0.5V	64.9	-0.66	1015.4	4.97e-5
		1V	65.2	-0.195		
		1.5V	64.2	0.345		
		2V	64.2	0.842		
	10^{19}	0.5V	98.6	0.8	1703.4	1.60e-4
		1V	120	1.31		
		1.5V	117	1.78		
		2V	125	2.32		
	10^{20}	0.5V	Not measureable	Not measureable	Not measureable	2.45e-3
		1V	Not measureable	Not measureable		
		1.5V	Not measureable	Not measureable		
		2V	Not measureable	Not measureable		

Table C.6: Data table of accumulation mode Si-NW transistors with NW thickness of 5nm.

Channel thickness	Doping concentration (cm^{-3})	Drain Voltage (v)	Subthreshold Slope (mv/dec)	Threshold voltage(v)	DIBL (mv/v)	Drive current (A/μm)
5nm	10^{14}	0.5V	61.15	-0.825	1000	4.82e-5
		1V	63.37	-0.3		
		1.5V	63.75	0.2		
		2V	62.04	0.6		
	10^{15}	0.5V	61.15	-0.825	1000	4.91e-5
		1V	63.37	-0.3		
		1.5V	63.75	0.2		
		2V	62.04	0.6		
	10^{16}	0.5V	61.15	-0.825	1000	4.9e-5
		1V	63.37	-0.3		
		1.5V	63.75	0.2		
		2V	62.04	0.6		

	10^{17}	0.5V	61.15	-0.825	1000	4.58e-5
		1V	63.37	-0.3		
		1.5V	63.75	0.2		
		2V	62.04	0.6		
	10^{18}	0.5V	61.92	-0.81	1022	4.04e-5
		1V	65.77	-0.275		
		1.5V	65.79	0.225		
		2V	64.49	0.725		
	10^{19}	0.5V	65.6	-0.25	1000	7.02e-5
		1V	67.33	0.25		
		1.5V	67.85	0.75		
		2V	67.48	1.25		
	10^{20}	0.5V	7552.3	Not measureable	4440	0.000954
		1V	7786.1	Not measureable		
		1.5V	8112.2	Not measureable		
		2V	8717.1	Not measureable		