PERFORMANCE COMPARISON OF GRAPHENE AND SILICON NANOWIRE TRANSISTORS

By

Atiqur Rahman,
Md. Rafeen Mannan, and
Md. Ifranul Islam

Submitted to the

Department of Electrical and Electronic Engineering
Faculty of Sciences and Engineering
East West University

In partial fulfillment of the requirements for the degree of
Bachelor of Science in Electrical and Electronic Engineering
(B.Sc. in EEE)

Spring 2012

Approved By

_____   _____

Thesis Advisor   Chairperson

Dr. Khairul Alam   Dr. Khairul Alam

Undergraduate Thesis

Abstract

Graphene nanoribbons and carbon nanotubes represent a novel class of low-dimensional materials. All these graphene based nanostructures are expected to exhibit the extraordinary electronic properties and therefore these are the promising candidates for a wide range of nanoscience and nanotechnology applications. So, in this work, the performance potential of ballistic graphene and silicon nanowire field effect transistors are examined for future high performance applications.

CNT is graphite sheet with a hexagonal lattice that has been wrapped up into a seamless cylinder. GNR consists of carbon atoms arranged in a 2-dimensional honeycomb crystal lattice. And rode like silicon crystals with a diameter of less than 100 nm is referred to as SiNW. These materials are being used as the channel materials of the transistors. In this work drain current I_D, transconductance g_m, number of mobile charge, quantum capacitance C_Q, gate capacitance C_G, gate delay τ and cut off frequency f_T of GNR, CNT and SiNW transistors have been calculated using ballistic top of the barrier model and then we plot those variables with respect to gate bias. To realize the performance of these three types of transistors, it is necessary to compare those characteristics with each other. On-current in carbon based channel is higher as well as I_{ON}/I_{OFF} is higher than SiNW channel due to lower effective mass. Higher on-current indicates sharper slope in current curve which ensures higher transconductance. So, CNT transistor has the highest transconductance. The density of states(DOS) of CNT and GNR transistors are lower than SiNW transistor. And the reason behind small gate capacitance is low density of states. On-current, transconductance and gate capacitance control the switching speed of a transistor. So from the simulations it seems that graphene transistors can be the candidates for future digital switches. But it is also important that SiNWs in particular are potentially very attractive, given the central role of silicon in the semiconductor industry and the existing set of known fabrication technologies.

Acknowledgements

First of all, we are grateful to the Almighty Allah for giving us the opportunity to complete the research.

We like to express sincere gratitude to our advisor Dr. Khairul Alam sir, Chairperson Department of Electrical and Electronic Engineering, East West University, for supervise overall project and guided throughout the course. Without his help and guidance this research could not be possible.

We also like to thank Dr. Anisul Haque sir and all the faculty members of Department of Electrical and Electronic Engineering, East West University for developing a concept about the research topic which is really helpful for doing this project.

Our heartfelt thanks to our parents is to guiding us and giving us courage each moment throughout our life.

Undergraduate Thesis

Authorization page

We hereby declare that we are the sole authors of this thesis. We authorize East West University to lend this thesis to other institutions or individuals for the purpose of scholarly research.

_____ _____ _____

Atiqur Rahman   Md. Rafeen Mannan   Md. Ifranul Islam

We further authorize East West University to reproduce this thesis by photocopy or other means, in total or in part, at the request of other institutions or individuals for the purpose of scholarly research.

_____ _____ _____

Atiqur Rahman   Md. Rafeen Mannan   Md. Ifranul Islam

Undergraduate Thesis

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1. INTRODUCTION

1.1. MOSFET Scaling

In modern integrated circuit it has been observed that MOSFET channel length changes in nanometer scale. The Si transistor in production today is below the 100 nm scale and has entered the nano electronics regime. Over last decade continuous scaling of silicon transistors has been the driving engine for the exponential growth of digital information processing systems.

Scaling limit in Si field-effect transistors (FETs) change on certain conditions. The main reason for reducing the space size of transistors is to pack more devices in smaller area. Increased number of transistor in a chip causes better device performance. The cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. More the chips are added in an IC, less is the cost. The number of transistors per chip has been doubled every 2–3 years once a new technology node is introduced over the past 30 years. This doubling of transistor density was first predicted by Gordon Moore in 1965 and is commonly referred to as Moore's law.

1.2. Scaling Behaviours in different Transistors

Scaling behavior in graphene nanoribbon has major changes compare with SI MOSFETs. Reducing the oxide thickness is more useful for improving transistor performance than using a high-κ gate insulator. When channel length scaled below 10 nm significant increase of the minimal leakage current is observed. This happens because small effective mass provides strong source drain tunneling. Scaling limit in Si MOSFETS is no longer followed in GNRFET. The intrinsic switching speed in GNR SBFET is several times faster than that of Si MOSFETs. And that could lead to promising high speed electronics applications in GNRFET where large number of leakage is no longer concerned. The total gate capacitance is limited by the semiconductor capacitance and it is no longer dependent on the gate insulator capacitance. The GNRFET has a one-dimensional channel with a monolayer of carbon atoms. It has small semiconductor capacitance which makes it to operate closer to the quantum capacitance limit compare with the Si FETs. The advantage to use multiple gate geometry is for the immunity to the short channel

effects. A thinner oxide therefore better for larger on current and on-off current ratio due to smaller sub threshold swing. Small size and low dimensional contacts not only improve the DC performance by increasing the on current, but also improve the AC performance by decreasing the parasitic capacitance between the electrodes, which leads to a higher operation speed. [1]

GNR and CNT are one-dimensional nanostructures and both derived from graphene. The scaling characteristics of GNR SBFETs show some similarities with CNT SBFETs. But the two types of transistors have some important difference. First, GNRFETs have different channel geometry leading to a different gate electrostatics. And a precise patterning technique could potentially lead to better control of defining channel material than CNTFETs. Second, due to the different quantum confinement in the transverse direction, an armchair edge GNR channel does not have valley degeneracy [2], which results in a smaller quantum capacitance. Compared to a CNT channel, it benefits even less from multiple gate structure. In addition, the edges of the GNR channel could potentially cause large potential variation in the transverse direction. The band gap of the GNR channel strongly depends on its width, which significantly affects the on current and off current. The larger on current found reducing the gate insulator thickness and contact size results thinner Schottky barriers. The intrinsic speed of the GNRFETs is several times faster than Si FETs due to its large carrier velocity and near ballistic transport, and reducing the parasitic capacitance results fast intrinsic speed [3].

1.3.   Silicon Nanowire

Silicon nanowires (SiNW) are the most perspective elements of nanotechnology. SiNW can be used in nanoelectronics as field-effect transistors, diodes, logic gates, and more. The structure and properties of silicon nanowires and nanorods under high pressure is almost a virgin field [4]. Research on silicon nanowires has developed rapidly in recent years. Rodlike crystals with a diameter of less than 100 nm will be referred to as nanowires. Regarding silicon wire growth, it is remarkable to see how much was already known in the 1960s. The best example of this is the vapor-liquid-solid mechanism of Si wire growth proposed by Wagner and Ellis in their seminal article published in March 1964. Till today, the vapor-liquid-solid (VLS) growth mechanism was the most prominent method for silicon wire synthesis [5].

Different techniques for silicon nanowire synthesis were developed with High Temperature Chemical Vapor Deposition, Low Temperature Chemical Vapor Deposition, Supercritical-Fluid-Based and Solution-Based Growth Techniques, Molecular Beam Epitaxy, Laser Ablation, Silicon Monoxide Evaporation [6]. Typically the diameter of the Si NWs vary from 3 to 10 nm, but by means of etching techniques diameters of about 1 nm can be achieved [6]. Silicon nanowires (SiNWs) in particular are potentially very attractive, given the central role of silicon in the semiconductor industry and the existing set of known fabrication technologies.

1.4. Carbon Nanotube

Carbon nanotubes can be considered as graphite sheets with a hexagonal lattice that has been wrapped up into a seamless cylinder. Since its discovery in 1991, the peculiar electronic properties of these structures have attracted much attention. Their electronic conductivity, for example, has been predicted to depend sensitively on tube diameter and wrapping angle with only slight differences in these parameters causing a shift from a metallic to a semiconducting state. In other words, similarly shaped molecules consisting of only one element (carbon) may have very different electronic behaviour. Although the electronic properties of multi-walled and single-walled nanotubes have been probed experimentally, it has not yet been possible to relate these observations to the corresponding structure. The bandgaps of both metallic and semiconducting carbon nanotube are consistent with theoretical predictions [7].

From early carbon nanotube experiments, owing to their molecular uniformity and quasi-one dimensional natures, it was expected that they would exhibit ballistic transport properties.It shows that carbon nanotube exhibit low temperature transport effects such as Coulomb blockade. However, further research is still required to determine experimentally their role in nanotube devices [8]. The mechanical properties are no less amazing and carbon nanotubes are simultaneously extremely strong and flexible fibres Due to this rather exceptional combination of properties, carbon nanotubes are now a model example of a robust 1- dimensional system. An additional advantage of nanotubes is that their extended lengths facilitate the use of standard electron beam lithography for device fabrication. In a carbon nanotube the electrons are free to move only in the length direction [9].

(A) (B)
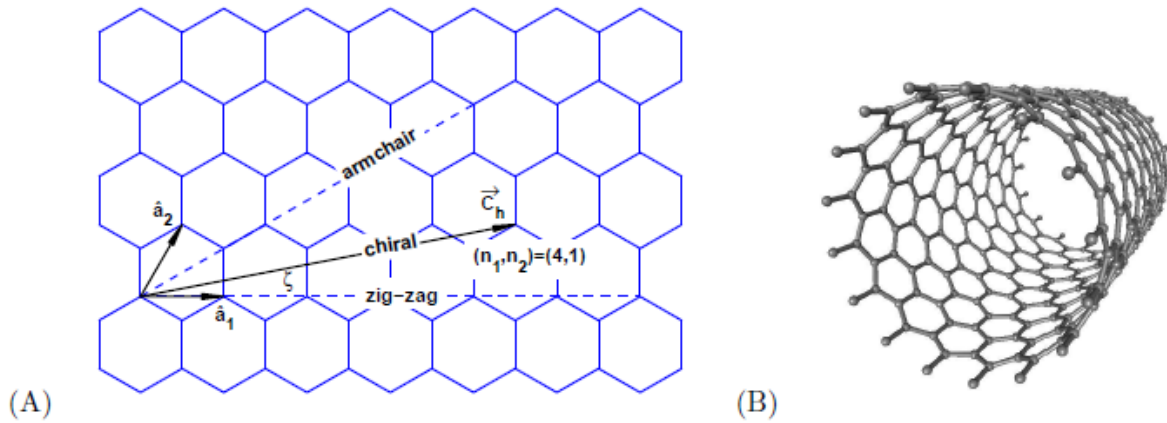
Figure 1-1:(A) 2D graphene with a few useful vectors (B) Rolled Carbon naotube lattice structures.

The CNT metal-oxide-semiconductor field-effect-transistor (MOSFET) has shown high performance, and is a possible candidate of a new channel digital logic switch. For realistic IC applications utilizing CNT MOSFETs, however, material properties such as the bandgap (*EG*) have to be precisely controlled. Although the bandgap of a CNT is a strong function of its chirality there is currently no straightforward way to control the CNT chirality during growth. Recent studies on carbon nano-ribbons show an alternative method to bypass the CNT chirality challenge and retain the excellent electronic properties of the graphene sheet such as light effective mass and high electron/hole mobility properties which appear in the CNTs [10].

Examples of the simple analytical solutions and the numerical results of the tight-binding model are shown on figure 1-2.

$$E_G(CNT) = \frac{0.8}{D_{CNT}} \; ; \text{ where } D_{CNT} \text{ is the diameter of carbon nanotube.}$$

If the width of an armchair GNR is the same as the outer boundary of a zigzag CNT, the bandgap of the CNT is approximately twice than that of the GNR. This occurs because of the two different boundary conditions that the structures encounter. The CNT sees a periodic boundary indicating as rapped up graphene, while GNR sees a hard wall boundary.
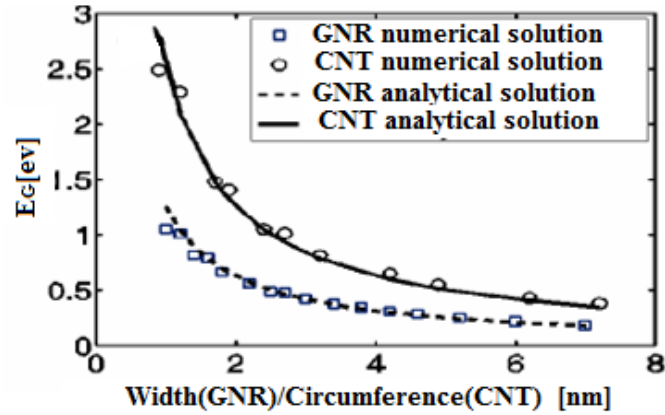
Figure 1-2: Comparisons of EG versus Width for GNRs and EG versus Circumference for CNTs for the simple analytical solutions and the numerical solutions (Gengachiau L et al., 2007 [10]).

1.5. Types of Carbon Nanotube:

There are different types of carbon nanotube observed over the last decades. Research material technology gets more attention on single walled and multiwalled carbon nanotube. Depending on the folding angle and the diameter, nanotubes can be metallic or semiconducting. So far, some experimental results of thermal conductivity for single-walled and multiwalled carbon nanotubes have been reported.Depending on the edge shape CNT divided in to two category, commonly known as armchair CNT and zigzag CNT.

SWNT   **MWNT**
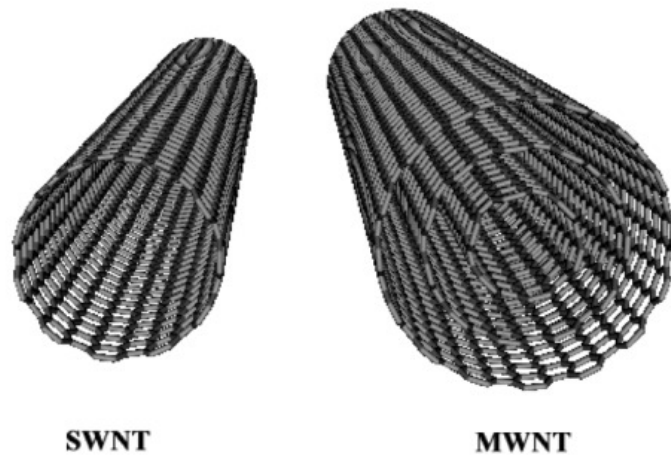
Figure 1-3:Single-walled and multi-walled carbon nanotube

Undergraduate Thesis

1.5.1. Single and Multi-walled carbon nanotube:

Single-walled carbon nanotubes (SWNTs) are nanometer-diameter cylinders consisting of a single graphene sheet wrapped up to form a tube. Since their discovery in the early 1990s, there has been intense activity exploring the electrical properties of these systems and their potential applications in electronics. Experiments and theory have shown that these tubes can be either metals or semiconductors shown in figure 1-4, and their electrical properties can rival, or even exceed, the best metals or semiconductors known [11].

SWNTs are grown by combining a source of carbon with a catalytic nanostructured material such as iron or cobalt at elevated temperatures. The carbon in the particle links up to form graphene and wraps around the catalyst to form a cylinder. Subsequent growth occurs from the continuous addition of carbon to the base of the tube at the nanoparticle or tube interface. SWNTs have remarkable electrical characteristics, making them a very promising new class of electronic materials [11].
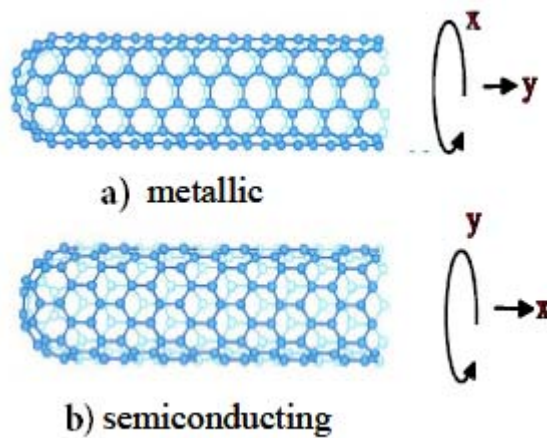
Figure 1-4:Graphene sheets rolled in to tubes, the results can be either a)metal or b)semiconductor

Multi-walled nanotubes (MWNT) consist of multiple rolled layers of graphene. There are two models that can be used to describe the structures of multi-walled nanotubes.Sheets of graphite are arranged in concentric cylinders, single-walled nanotube (SWNT) within a larger single-walled nanotube. In the Parchment model, a single sheet of graphite is rolled in around itself, resembling a scroll of parchment or a rolled newspaper. The interlayer distance in multi-

walled nanotubes is close to the distance between graphene layers in graphite, approximately 3.4 Å [12].

The multiwall carbon nanotubes are primarily used as a well-defined model system and the observed transport characteristics are not nanotube specific but generic features of many mesoscopic devices. These include electron interference phenomena, quantum dot physics, and the effect of superconducting proximity.

1.5.2. Armchair and Zigzag CNT

The deformation of armchair single-walled carbon nanotube under transverse electric field has been investigated using density functional theory. The results show that the circular cross-sections of the nanotubes are deformed to elliptic ones, in which the tube diameter along the field direction is increased, whereas the diameter perpendicular to the field direction is reduced. The electronic structures of the deformed nanotubes were also studied. The ratio of the major diameter to the minor diameter of the elliptic cross-section was used to estimate the degree of the deformation. It is found that this ratio depends on the field strength and the tube diameter. However, the field direction has little role in the deformation [13].

All finite zigzag CNTs possess a spin-polarized ground state with a long-range antiferromagnetic-type spin ordering. This state is characterized by high spin density of opposite spins located at the two zigzag edges of the molecule. The energy gap between the highest occupied and the lowest unoccupied molecular orbital of the finite systems is found to be inversely proportional to the nanotube's segment lengths, suggesting a route to control their electronic properties [14].

1.6. Graphene Nanoribbon

Graphene allows enormous research since its experimental discovery in 2004. It consists of carbon atoms arranged in a 2-dimensional honeycomb crystal lattice with a bond length of 1.42 Å. Two types of graphene nanoribbon are found considering on edge shapes one is armcair GNR and another is zigzag GNR. Graphene sheets can be processed with conventional CMOS-technology is potentially a huge advantage over CNTs[15]. Two-dimensional graphene is a zero gap material, which does not suitable for transistor applications. Energy gap can however be

induced by means of lateral confinement, for example which include by lithography definition of narrow graphene stripes called Graphene Nanoribbons. Recent theoretical works have shown that graphene nanoribbons have an energy gap which has an oscillating behaviour as a function of width, with average roughly proportional to the inverse width, and that edge states play a very important role in inhibiting the existence of fully metallic nanoribbons [16].

Researchers view over graphene nanoribbon shows a promising new material for electronic, chemical, or electromechanical applications, where graphene's unique properties may be of substantial benefit. Furthermore, the Dirac energy dispersion in 2D implies that graphene is a gapless semiconductor, whose density of states vanishes linearly when approaching the Fermi energy. Depending on the operating regime, graphene can be pushed in either direction. For example, it is possible to open a gap in a sample with the help of chemical modifications, or lateral confinement one can make graphene metallic, by chemical doping [17].

.

Graphene is, of course, known to be a semimetal, but the spatial confinement of the ribbons in their transverse direction can induce a bandgap. The width of the ribbon and its transport orientation relative to the graphene crystal structure are the two parameters that determine the bandgap and the electronic properties of the GNR in a similar way that the chirality controls the properties of the CNT [18].

The relations between E_G (band gap) and width of armchair GNRs can be derived as following [10],

$$E_G (GNR) = 0.8 \frac{\pi}{2 W_{GNR}} ; \text{ where } W_{GNR} \text{ is the width of graphene nanoribbon.}$$

1.7. Types of GNR

GNRs are obtained by defining a lateral confinement in graphene. This is done by confining the width of graphene, so that it forms a long, narrow ribbon. Therefore, GNRs are a one dimension (1D) structure with confinement of carriers in two directions. GNRs are classified according to their edges. The carbon atoms on the edge of GNRs have two typical topological shapes.
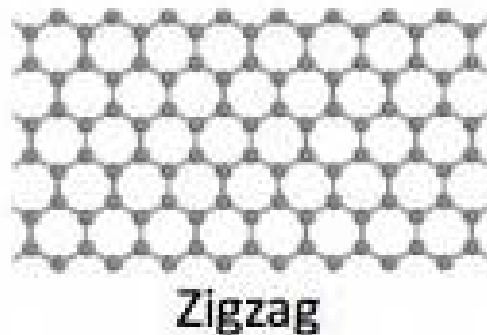
1. Zigzag.

2. Armchair.

The names armchair and zigzag named after their characteristic appearance on the atomic scale and follow the standard GNR literature convention, which is opposite to the CNT(carbon nanotube) convention .

1.7.1. Zigzag GNR

The edge sites are emphasized by solid circles on each side. Perpendicular to the direction of defined width, GNRs repeat their geometric structures, and form one-dimensional periodic structures. Since GNRs are stripes of graphene, edge atoms are not saturated. Therefore, active edge states become an important factor to determine the edge structures. For zigzag GNRs, it was unexpectedly found that the zigzag edge (figure 1-5) is metastable, and reconstruction spontaneously takes place at high temperature. The width of zigzag GNR plays an important role. The electronic properties of zigzag graphene nanoribbons (Z-GNRs) adsorbed on Si substrate strongly depend on ribbon width.

Figure 1-5: Edges of Zigzag GNR

The width of a zigzag ribbon is now identified with the number of zigzag chains N [19],

$$Wzz = (N-1)\frac{3}{2} a \qquad \text{with } a = 1.42\text{Å nearest neighbor distance}$$

1.7.2. Electron Transport in Zigzag GNR

Tailored from monolayer graphene, graphene nanoribbon (GNR) with finite width has been shown to hold unusual electronic properties depending on their edge shape and width. Based on these earlier studies all zigzag GNRs (ZGNRs) were predicted to be metallic,

while AGNRs were grouped into semiconducting and metallic character. The metallic character of ZGNRs was attributed to the presence of a high density of edge states at the Fermi level. The zigzag edges present electronic localized states at the boundaries, corresponding to non-bonding states that appear at the Fermi level as a large peak in the density of states. Phenomena related to magnetic and spin properties arising due to specific edge structure of graphene ribbons have also been investigated theoretically. Due to the non-bonding character of the zigzag localized edge states, the geometrical reconstruction is unlikely to happen and the spin polarization of the electronic density establishes an anti-ferromagnetic arrangement (Figure 1-6) with the opening of a gap, yielding a Slater insulator [20] .
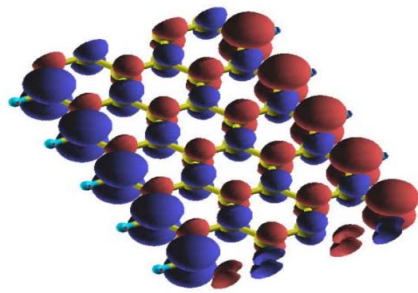
Figure 1-6:Spin density map, showing the anti-ferromagnetic arrangement between opposite edges (Ricardo F et al., 2009 [20]).

In more detail, graphene nanoribbons with zigzag edges (ZGNRs) possess spin polarized peculiar edge states and spin polarized electronic state provides half metallicity under transverse electric field and has great potential in the application as spintronics . It is mainly attributed that an in plane electric field, perpendicular to the periodic axis, induces a half metal state in zigzag nanoribbons (ZGNR). Apart from the interesting dependence of the electronic structure upon an electric field, this is a promising material for future spintronic devices, since it could work as a perfect spin filter.

1.7.3.   Armchair GNR

The edge sites are emphasized by solid circles on each side. Perpendicular to the direction of defined width, GNRs repeat their geometric structures, and form one-dimensional periodic structures. Since GNRs are stripes of graphene, edge atoms are not saturated. Therefore, active edge states become an important factor to determine the edge structures. For armchair GNRs (figure 1-7), there is no edge reconstruction, and the planar patterns are kept.
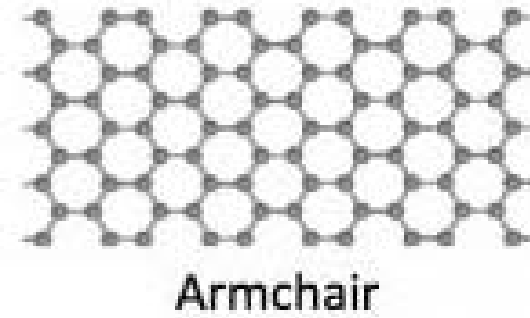
Figure 1-7:Edges of Armchair GNR

The width of an armchair ribbon can be defined in terms of the number of dimer lines [7]

$$Wac = (N-1)\frac{\sqrt{3}}{2} \, a \qquad \text{with a = 1.42Å nearest neighbor distance}$$

1.7.4. Electron Transport in Armchair GNR

Many theoretical studies have been devoted into investigating the electronic properties of armchair GNRs, such as tight-binding calculations, density functional theory (DFT) calculations, and many-electron green's function approach. Among those methods, DFT calculations adopt parameter free self consistent field calculations, and their reliability has been broadly proved in solid state field and nano-scale systems. Thus, most of the theoretical investigations have been carried out with DFT calculations. However, it is well established that DFT calculations underestimate band gaps. Other methods, such as tight-binding calculations, have been adapted to correct DFT calculations, and get the reliable band gaps.

Armchair GNRs show semiconducting behaviors with a direct energy gap. The determining factor comes from the quantum confinement effect (QCE), which can be characterized by energy gaps is inverse of width. Besides the QCE, researchers have pointed that the edge effects play an important role to force the armchair GNRs to be semiconductors . As shown in figure 1-8, the edge of carbon atoms of armchair GNRs are usually passivated by hydrogen atoms, which lead to the bonding of carbon atoms at the edges different with other carbon atoms. As a consequence, the bond lengths of carbon atoms at the edges are shorter than that in the middle of ribbons, and open the energy gaps of armchair GNRs. Although armchair GNRs have three typical families (corresponding to N = 3p,

3p+1, 3p+2, respectively, where p is any integer) with distinguished energy gaps, they have similar band shapes [10].
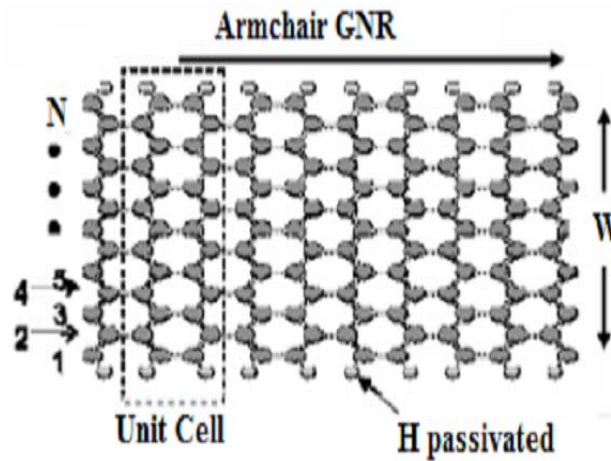
Figure 1-8:Atomic structure of an armchair GNR (Gengachiau L et al., 2007 [11]

1.8. Objectives of the Project

The main purpose of our thesis is to study the performance comparison of silicon nanowire and graphene transistors. Then realize the electrical characteristics of GNRFET and compare those characteristics with the electrical characteristics of CNTFET and SiNWFET. At the end, we explore and study the role of GNRFET in future electronic system.

2. TOP OF THE BARRIER MODEL

The model takes the band structures of GNRs as an input and it has previously been applied to model silicon nanoscale MOSFETs, nanowire FETs, and CNTFETs. This model provides insights into the performance of MOSFETs near the scaling limit, and a unified framework for assessing and comparing a variety of novel transistors. The model assesses the performance limits by assuming (i) the channel is ballistic (no scattering), and (ii) the transistor contacts are ideal (with a perfect transmission).To derive the top of the barrier model we are following theoretical issues that provided in Fundamentals of Nanotechnology course. Related issues are given below,

2.1.1. DATTA ToyFET:

In a single energy model of a ToyFET that includes the contact-device coupling and then extend it to the single sub-band model. The ToyFET model was originally proposed by prof. Supriyo Datta of Purdue University to understand the transport mechanism of molecular transistors. Let us consider a simple picture shown below. The device part is represented by a single energy level $\in$
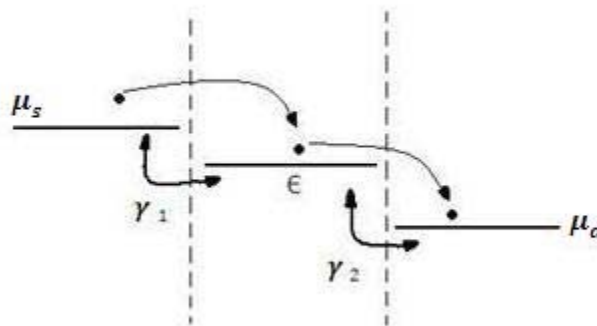

Figure 2-1:Fermi Energy level in ToyFET

The source contact is characterized by a Fermi level μ_s and the drain contact by μ_d.At equilibrium, both the source and drain Fermi levels align and therefore no current flows. Now if we apply a drain bias then μ_s-μ_d=eV_{ds} and an energy window is created for current to flow.

Undergraduate Thesis

However, if the energy level of ϵ is not between μ_s and μ_d then no current will flow. Under that situation, we have to apply the gate bias to bring the energy level ϵ in the energy range between μ_s and μ_d for the current to flow. Now the source contact will inject electron and try to fill the energy level ϵ and the drain contact will try to empty it out. Therefore, a balance between filling up and emptying out will be established and current will flow. If N_1 is the average number of electrons that the left contact would like to see at the channel then

$$N_1 = 2f(\epsilon - \mu_s) = \frac{2}{1 + e^{\frac{(\epsilon - \mu_s)}{kT}}} \qquad \text{........ [2.1]}$$

Here the factor of 2 includes spin degeneracy. Similarly the average number of electrons N_2 that the drain contact would like to see at the channel is

$$N_2 = 2f(\epsilon - \mu_d) = \frac{2}{1 + e^{\frac{(\epsilon - \mu_d)}{kT}}} \qquad \text{.......... [2.2]}$$

However, the average number of electrons at the channel is N at stead-state. Therefore, N_1-N is the average number of electrons that are pumped in to channel from the source contact.

2.1.2. Single Sub-band Ballistic Model

The transport in most of the nanostructures such as carbon nanotubes, silicon nanowires is ballistic in the ultimate scaling limit. The ballistic current has both the tunneling and the thermionic components. Here an analytical model is derived for the I-V characteristics of nano devices under single sub-band approximation. The current is thermionic only in the derivation. The Landaur equation for ballistic current is

$$I = \frac{2e}{h} \int_{E_C - e\varphi_s}^{\infty} dE\, T(E) [f(E - \mu_s) - f(E - \mu_d)] \qquad \text{..........[2.3]}$$

Here e is the electron charge, h is Planck's constant, T(E) is the transmission coefficient, f is the Fermi distribution function, μ_S and μ_D are the source and drain Fermi levels, respectively,

and the factor of 2 accounts for spin degeneracy. The integration is performed from the bottom of conduction band to infinity for electron current. The conduction band bottom without gate bias is E_C and ψ_S is the surface potential. For thermionic emission current T(E)=1, and the current becomes

$$I = \frac{2e}{h} \int_{E_c - e\varphi_s}^{\infty} dE \left[\frac{1}{1 + e^{\frac{E - \mu_s}{kT}}} - \frac{1}{1 + e^{\frac{E - \mu_d}{kT}}} \right] \quad ....[2.4]$$

Now integration of $\int \frac{dE}{1 + e^{\frac{(E - \mu_s)}{kT}}}$ becomes $- kT \ln(1 + e^{\frac{(\mu_s - E)}{kT}})$. Therefore, the current expression becomes

$$I = \frac{-2ekT}{h} \left\{ \left[\ln \left(1 + e^{\frac{(\mu_s - E)}{kT}} \right) \right]_{E_c - e\varphi_s}^{\infty} - \left[\ln \left(1 + e^{\frac{(\mu_d - E)}{kT}} \right) \right]_{E_c - e\varphi_s}^{\infty} \right\} \quad .....[2.5]$$

Now putting values in the above expression, we get the current as the following

$$I = \frac{2ekT}{h} \left[\ln \left(1 + e^{\frac{(\mu_s + e\varphi_s - E_C)}{kT}} \right) - \left[\ln \left(1 + e^{\frac{(\mu_d + e\varphi_s - E_C)}{kT}} \right) \right] \right] \quad ....[2.6]$$

The first term in the expression of current is the forward term that dominates in the saturation and the second term is the backward term that dominates in the linear region.

$$\text{Now, } I = \frac{2ekT}{k} \left[\ln \left(1 + e^{\frac{(\mu_s - (E_C - e\varphi_s))}{kT}} \right) - \left[\ln \left(1 + e^{\frac{(\mu_d - (E_C - e\varphi_s))}{kT}} \right) \right] \right] \quad .....[2.7]$$

Here, $E_C = \frac{E_g}{2}$; for undoped channel with reference energy $E_F = 0$

$$U_{top} = \frac{E_g}{2} - e\varphi_s$$

$$\text{So, } I = \frac{2ekT}{h} \left[\ln \left(1 + e^{\frac{(\mu_s - U_{top})}{kT}} \right) - \left[\ln \left(1 + e^{\frac{(\mu_d - U_{top})}{kT}} \right) \right] \right] \quad ....[2.8]$$

Undergraduate Thesis

$$\text{Or, } I = (2)\ \frac{2qkT}{h}\ \ln\left[\frac{1+\exp\left(\frac{\mu_s-U_{top}}{kT}\right)}{1+\exp\left(\frac{\mu_d-U_{top}}{kT}\right)}\right] \quad \text{........ [2.9]}$$

For sub-band degeneracy, 2 is multiplied with current equation.

2.1.3. Surface potential

In the derivation of current, we have quantity φ_s called surface potential. The current expression is derived assuming a single point as the channel, where the potential barrier along the source to drain is highest, and the transmission coefficient is unity above it and zero below it. This point of the channel is electro statically connected to the gate, to the source, and to the drain that can be schematically represented as shown below,
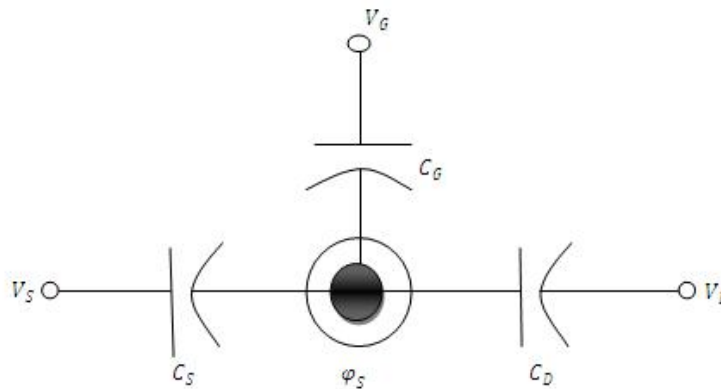
Figure 2-2:The potential at the top of the barrier is controlled by the gate, drain, and source potentials through the three capacitors.

Now the expression of charge above equilibrium at that channel point would be the balanced by the charge associated with the three capacitors as follows,

$$e(N-N_o) = C_G(V_G-\varphi_s) + C_S(V_s-\varphi_s) + C_D(V_D-\varphi_s) \quad \text{..........[2.10]}$$

Now we can rearrange the terms to solve for the surface potential as follows

Undergraduate Thesis

$$\varphi_s = \alpha_g V_G + \alpha_s V_S + \alpha_d V_D - \frac{e(N - N_0)}{C_T} \qquad \text{........ [2.11]}$$

Where $\alpha_g = \frac{C_G}{C_T}$ is the gate control parameter, $\alpha_s = \frac{C_S}{C_T}$, and $\alpha_d = \frac{C_D}{C_T}$ and $C_T = C_G + C_S + C_D$ is the total capacitance. The term $\frac{e(N - N_0)}{C_T}$ is related to the quantum capacitance. When a device operates in the quantum capacitance limit, then α_g becomes unity and $\alpha_s = \alpha_d = 0$. To calculate the surface potential φ_s, we need to know N the total number of electron at the channel ($N_0 = N$ at equilibrium i.e $\varphi_S = 0$). The total number of electron can be obtained by integrating the DOS function times the quasi Fermi function in energy. However, we do not know the quasi Fermi function in the channel; rather we know the two Fermi levels, μ_S and μ_D. How the channel states are populated by the carriers according to these two Fermi levels are shown in the following figure.
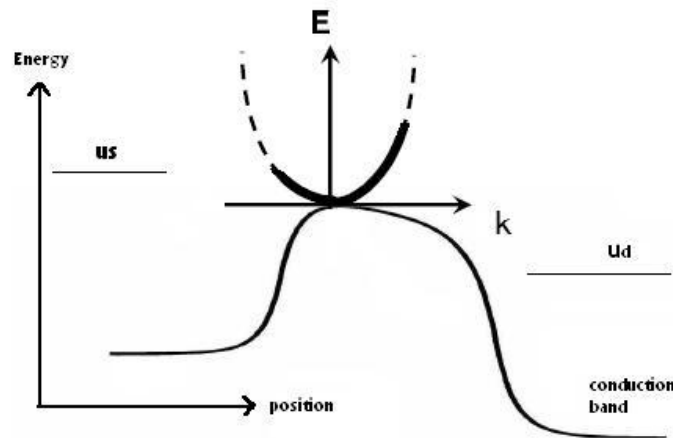
Figure 2-3:k states at the top of the barrier insert by two fermi level

The electrons that are injected from the left (source) contact have positive velocity .Therefore, the right half(positive k) of E-k relation will be filled up by the carriers according to the source Fermi level. Similarly the left moving electrons will fill up the negative k states according to the drain Fermi level. Now if we approximate the local density of states by bulk expression, then half of the bulk DOS will be associated with the source and next half with the drain (E-k is symmetric).However, at equilibrium the two Fermi levels are equal (Ef) and N_o can be obtained from the following equation.

Undergraduate Thesis

$$N_0 = \int_{E_C}^{\infty} \left(\frac{1}{\pi\hbar}\sqrt{\frac{2m^*}{E-E_C}}\right) \frac{1}{1+\exp\left(\frac{E-E_f}{kT}\right)} dE \quad ....[2.12]$$

Note that the expression does not contain channel length L, because we are calculating the density of electrons not the actual number of electrons.

Now the positive moving electrons N^+ and the negative moving electrons N^- can separately be calculated according to the following equation and $N = N^+ + N^-$.

$$N^+ = \int_{U_{top}}^{\infty} \frac{1}{2\pi\hbar}\sqrt{\frac{2m^*}{E-U_{top}}} \frac{1}{1+\exp\left(\frac{E-\mu_1}{kT}\right)} dE \quad ......[2.13]$$

$$N^- = \int_{U_{top}}^{\infty} \frac{1}{2\pi\hbar}\sqrt{\frac{2m^*}{E-U_{top}}} \frac{1}{1+\exp\left(\frac{E-\mu_2}{kT}\right)} dE \quad ....[2.14]$$

Here we use $U_{top} = \frac{E_g}{2} - \varphi_S$.

2.2. Necessary Equations

The code is written in Matlab to self-consistently calculate U_{top} and N

We know Ballistic MOSFET current

$$I = (2)\frac{2qkT}{h} \ln\left[\frac{1+\exp\left(\frac{\mu_1-U_{top}}{kT}\right)}{1+\exp\left(\frac{\mu_2-U_{top}}{kT}\right)}\right] \quad ......[2.15]$$

Also We know Doping Concentration of Source,

$$N_{1D} = 2\int_0^{\infty} D(E)\ f(E,\mu_1)\ dE \quad ....[2.16]$$

Where Density of States for 1D, $D(E) = \frac{\sqrt{2m^*}}{\pi\hbar} E^{-\frac{1}{2}}$

Undergraduate Thesis

$$So,\ N_{1D} = \frac{2\sqrt{2m^*}}{\pi h} \int_0^\infty \frac{E^{-\frac{1}{2}}}{1+\exp\left(\frac{E-\mu_1}{kT}\right)}\ dE \quad ....\ [2.17]$$

From Fermi-dirac integral we found,

$$F_j(x) = \frac{1}{\Gamma(j+1)} \int_0^\infty \frac{t^j}{1+\exp(t-x)}\ dt \quad ......\ [2.18]$$

Let, $\frac{E}{kT} = t$

or, $dE = KT\ dt$

or, $E^{-\frac{1}{2}} = (kT)^{-\frac{1}{2}} t^{-\frac{1}{2}}$

$$So,\ N_{1D} = \frac{2\sqrt{2m^*kT}}{\pi h} \int_0^\infty \frac{t^{-\frac{1}{2}}}{1+\exp\left(t-\frac{\mu_1}{kT}\right)}\ dt \quad ......\ [2.19]$$

$$= \frac{(\sqrt{\pi})2\sqrt{2m^*kT}}{\pi h} \left[\left(\frac{1}{\sqrt{\pi}}\right) \int_0^\infty \frac{t^{-\frac{1}{2}}}{1+\exp\left(t-\frac{\mu_1}{kT}\right)}\ dt\right] \quad ....\ [2.20]$$

$$So, N_{1D} = \frac{2}{h} \sqrt{\frac{2m^*kT}{\pi}}\ F_{-\frac{1}{2}}\left(\frac{\mu_1}{kT}\right) \quad ....\ [2.21]$$

Here N_{1D} is given

From this equation we will find out the value of μ_1

$\mu_2 = \mu_1 - qV_{ds}$

Now, $U_{top} = \frac{Eg}{2} - \varphi_s$; (Here Eg in ev)

Where, $E_g = \frac{0.8}{d}$

For GNR $d = \frac{2W}{\pi}$,where W is width of GNR

$$\varphi s = \alpha_g V_{gs} + \alpha_d V_{ds} - \frac{q\Delta n}{C_T} \quad ....[2.22]$$

given that, $\alpha_g = 0.88$, and $\alpha_d = 0.04$

$$C_T = \frac{cox}{\alpha_g} \quad ....[2.23] \quad ;$$

$$\text{where, } cox = \frac{2\pi + \varepsilon_0 + \varepsilon_{ox}}{\ln\left(1 + \frac{2t_{ox}}{d}\right)} \quad ....[2.24]$$

Here,d is diameter of CNT/Si Nwire

Now $\Delta n = N - No$

$$N = N^+ + N^- \quad ....[2.25]$$

Here, $N^+ =$ Positive moving electron

   $N^- =$ Negative moving electron

$$N^+ = \int_{U_{top}}^{\infty} \frac{1}{2\pi\hbar} \sqrt{\frac{2m^*}{E - U_{top}}} \frac{1}{1 + \exp\left(\frac{E - \mu_1}{kT}\right)} dE \quad ......[2.26]$$

$$N^- = \int_{U_{top}}^{\infty} \frac{1}{2\pi\hbar} \sqrt{\frac{2m^*}{E - U_{top}}} \frac{1}{1 + \exp\left(\frac{E - \mu_2}{kT}\right)} dE \quad ....[2.27]$$

Let, $t = \frac{E - U_{top}}{kT}$

or, $kT\, dt = dE$

$$\frac{E}{kT} = t + \frac{U_{top}}{kT}$$

From equation (2.25),

$$N = \frac{\sqrt{2m^*}}{2\pi\hbar} \left[\int_0^\infty \frac{t^{\frac{1}{2}}}{\sqrt{kT}} \; \frac{kT\,dt}{1 + \exp\left(t + \frac{U_{top}}{kT} - \frac{\mu_1}{kT}\right)} + \int_0^\infty \frac{t^{\frac{1}{2}}}{\sqrt{kT}} \; \frac{kT\,dt}{1 + \exp\left(t + \frac{U_{top}}{kT} - \frac{\mu_2}{kT}\right)} \right] \quad \dots\dots \; [2.28]$$

let, $\eta_s = \frac{\mu_1 - U_{top}}{kT}$ and $\eta_d = \frac{\mu_2 - U_{top}}{kT}$

$$\text{So, } N = \frac{\sqrt{2m^*kT}}{2\pi\hbar} \left[\sqrt{\pi}\frac{1}{\sqrt{\pi}} \int_0^\infty \frac{t^{-\frac{1}{2}}}{1 + \exp\,(t - \eta_s)} \, dt + \sqrt{\pi}\frac{1}{\sqrt{\pi}} \int_0^\infty \frac{t^{-\frac{1}{2}}\,dt}{1 + \exp\,(t - \eta_d)} \right] \quad \dots\dots[2.29]$$

$$\text{or, } N = \frac{\sqrt{2m^*kT}}{2\pi\hbar} \sqrt{\pi} \left[\frac{1}{\sqrt{\pi}} \int_0^\infty \frac{t^{-\frac{1}{2}}}{1 + \exp\,(t - \eta_s)} \, dt + \frac{1}{\sqrt{\pi}} \int_0^\infty \frac{t^{-\frac{1}{2}}\,dt}{1 + \exp\,(t - \eta_d)} \right] \quad \dots\dots[2.30]$$

From Fermi-dirac Integral equation we can write,

$$N = \frac{1}{2\hbar} \sqrt{\frac{2m^*kT}{\pi}} \left[F_{-\frac{1}{2}}(\eta_s) + F_{-\frac{1}{2}}(\eta_d) \right] \quad \dots\dots[2.31]$$

If sub-band degeneracy =2

Undergraduate Thesis

$$N = \frac{2}{2h}\sqrt{\frac{2m^*kT}{\pi}}\left[F_{-\frac{1}{2}}(\eta_s) + F_{-\frac{1}{2}}(\eta_d)\right] \qquad \text{........ [2.32]}$$

$$= \frac{1}{h}\sqrt{\frac{2m^*kT}{\pi}}\left[F_{-\frac{1}{2}}(\eta_s) + F_{-\frac{1}{2}}(\eta_d)\right] \qquad \text{........ [2.33]}$$

At equilibrium the two Fermi levels are equal and N_0 can be obtained from, the following equation,

$$N_0 = \frac{1}{h}\sqrt{\frac{2m^*kT}{\pi}}\left[F_{-\frac{1}{2}}(\eta_{s0}) + F_{-\frac{1}{2}}(\eta_{d0})\right] \qquad \text{.......[2.34]}$$

Where, $\eta_{s0} = \dfrac{u_1 - \frac{Eg}{2}}{kT}$, $\eta_{d0} = \dfrac{u_2 - \frac{Eg}{2}}{kT}$

And $u_1 = u_2$

From the equation of U_{top},

$$U_{top} - \frac{Eg}{2} + \psi_s - 0 \qquad \text{...... [2.35]}$$

$$\text{or,} \, U_{top} - \frac{Eg}{2} + \alpha g V_{GS} + \alpha d V_{DS} - \frac{q\Delta n}{CT} = 0 \qquad \text{..........[2.36]}$$

From this equation we will obtain various values of U_{top} for various values of V_{GS} and V_{DS}

$$g_m = \frac{dI}{dV_G} \qquad \text{.......[2.37]}$$

Gate capacitance relation can be obtained from a capacitive network as shown below,
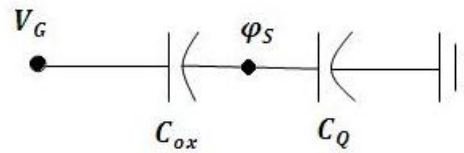
Figure 2-4: Gate Capacitive Network

$$\frac{1}{C_g} = \frac{1}{C_{ox}} + \frac{1}{C_q} \qquad \ldots\ldots\ldots [2.38]$$

$$\text{or, } C_g = \frac{C_{ox} \times C_q}{C_{ox} + C_q} \qquad \ldots\ldots [2.39]$$

Now, $Cq = \frac{dQ}{d\varphi_s}$; where $Q = q\Delta n$

      Once the gate capacitance, the on-state current, and the transconductance and know, we can calculate the switching delay and the cut-off frequency as following,

$$\tau = \frac{C_g V_{DD}}{I_{on}} \qquad \ldots\ldots\ldots [2.40]$$

$$f_T = \frac{g_m}{2\pi C_g} \qquad \ldots\ldots [2.41]$$

where , $V_{DD} = 0.5V$

From the ITRS of 2011 we obtain, $I_{off} = 1 \times 10^{-8}A$

3. RESULTS AND DISCUSSION

This research involves simulation study to investigate the I-V characteristic of graphene and silicon nanowire transistors. The simulation study is carried out using MATLAB based on single subband top of the barrier model [16]. Three kinds of devices have been investigated for their performance based on a common off-current. The ballistic top of the barrier model is used to evaluate the current voltage characteristics. Finally, the results are interpreted and conclusions are drawn based on the obtained results. The model takes the band structures and the effective mass as inputs. The model assesses the performance limits by assuming (i) the channel is ballistic (no scattering), and (ii) the transistor contacts are ideal (with a perfect transmission).

Therefore, upon comparing GNR, CNT and SiNW devices, factors such as the bandgap and the fact that a certain diameter CNT has a larger conducting circumference than a GNR of the same width should be taken into consideration. In all simulations, off-current is set to 10nA and the thickness of high-k dielectric material is 3 nm. So in this work, we compare a GNR having a width close to the circumference of the 1.5 nm CNT and SiNW. The parameters used for simulation are listed in Table 3-1.

Table 3-1: List of parameters used in simulation

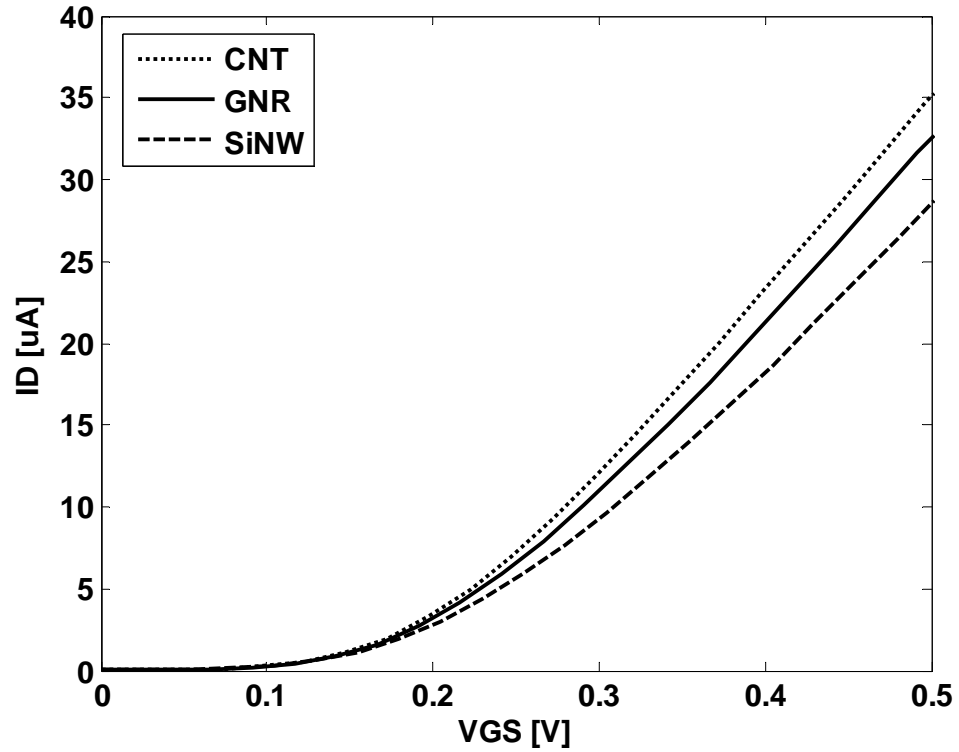| Parameter	D/W [nm]	$m_t(m_0)$	E_g [eV]	N_{1D} [1/nm]
CNT	1.5	0.05	0.53	0.2
GNR	4.2	0.08	0.3	0.2
SiNW	1.5	0.19	1.12	0.2

Figure 3-1: I_D versus V_{GS} characteristics of three types of transistors at V_{DS}=0.5V
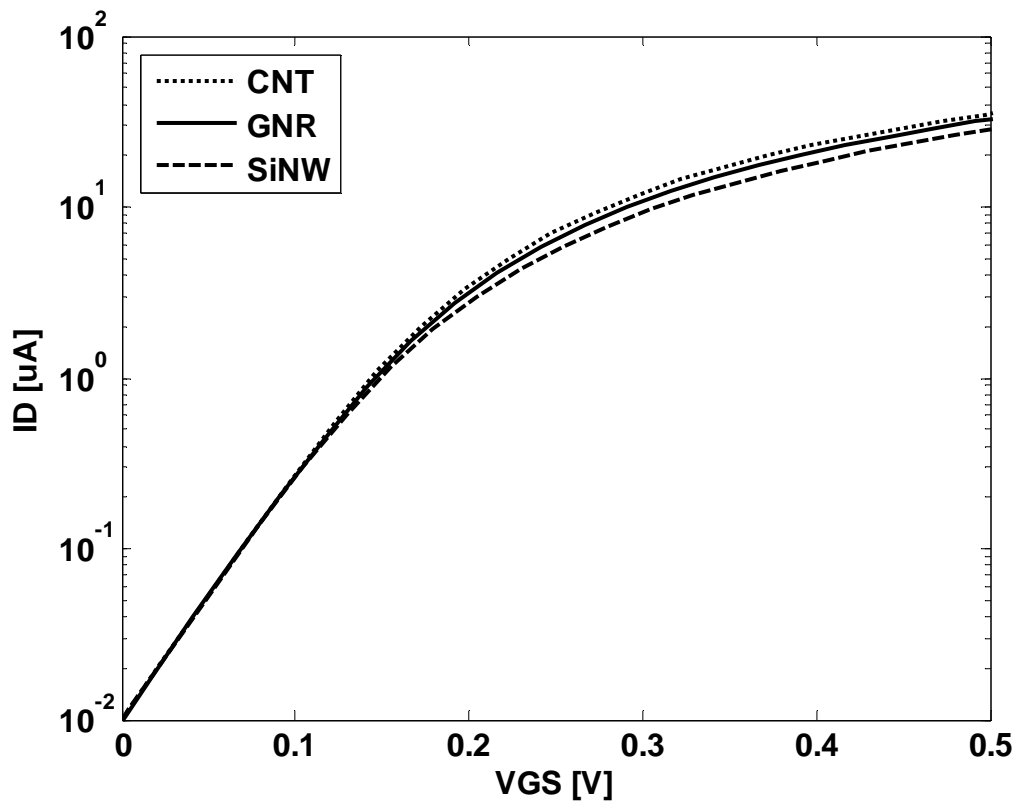

Figure 3-2: I_D versus V_{GS} characteristics of three types of transistors at V_{DS}=0.5V (in log scale)

When the width of conducting graphene increases, the number of carriers involved in transport increases. It is therefore, more appropriate to compare the on-current of a grapheme nanoribbon whose width is closer to the circumference of 1.5 nm diameter CNT and SiNW. Figure 3-1 and 3-2 show the drain current versus gate bias plots for a drain bias of 0.5V. In these plots, V_{GS}=0 is corresponding to a drain current of 10nA. As shown in figure 3-1 and 3-2, the on current of wider GNR show a slight improvement against the SiNW which has the same diameter as CNT. We generated an I_D versus V_{GS} curve for each transistor. In figure 3-1, the on-current of CNT, GNR and SiNW are 35.1μA, 32.6μA and 28.3μA. The higher on-current in carbon based channel is due to lower electron effective mass. Recall that off-current is common for every transistor, so I_{ON}/I_{OFF} of GNR is less than CNT but greater than SiNW.
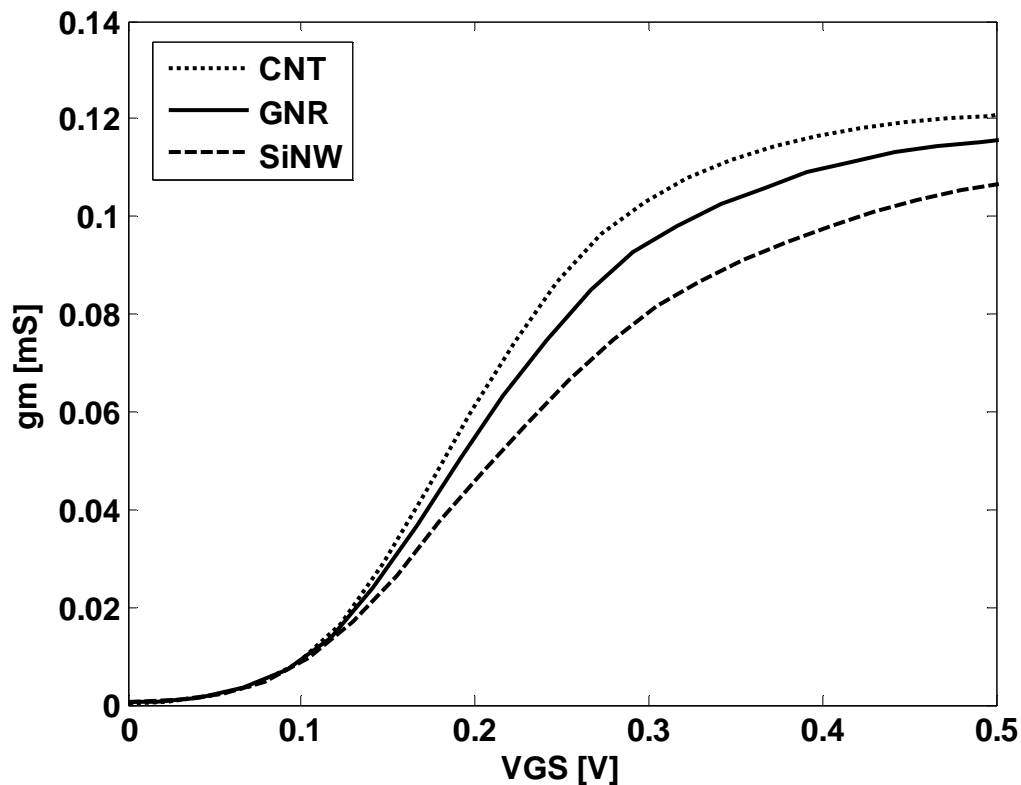

Figure 3-3: g$_m$ versus V$_{GS}$ characteristics of three types of transistors at V$_{DS}$=0.5V

Figure 3-3 shows the transconductance versus gate bias plots for a drain bias of 0.5V. From figure 3.3 we observe that at V_{ON} the magnitude of transconductance of CNT, GNR and SiNW transistors are 0.121mS, 0.115mS and 0.107mS. So the transconductance of CNT transistor is higher than GNR transitor and the transconductance of GNR transistor is higher than SiNW transistor.
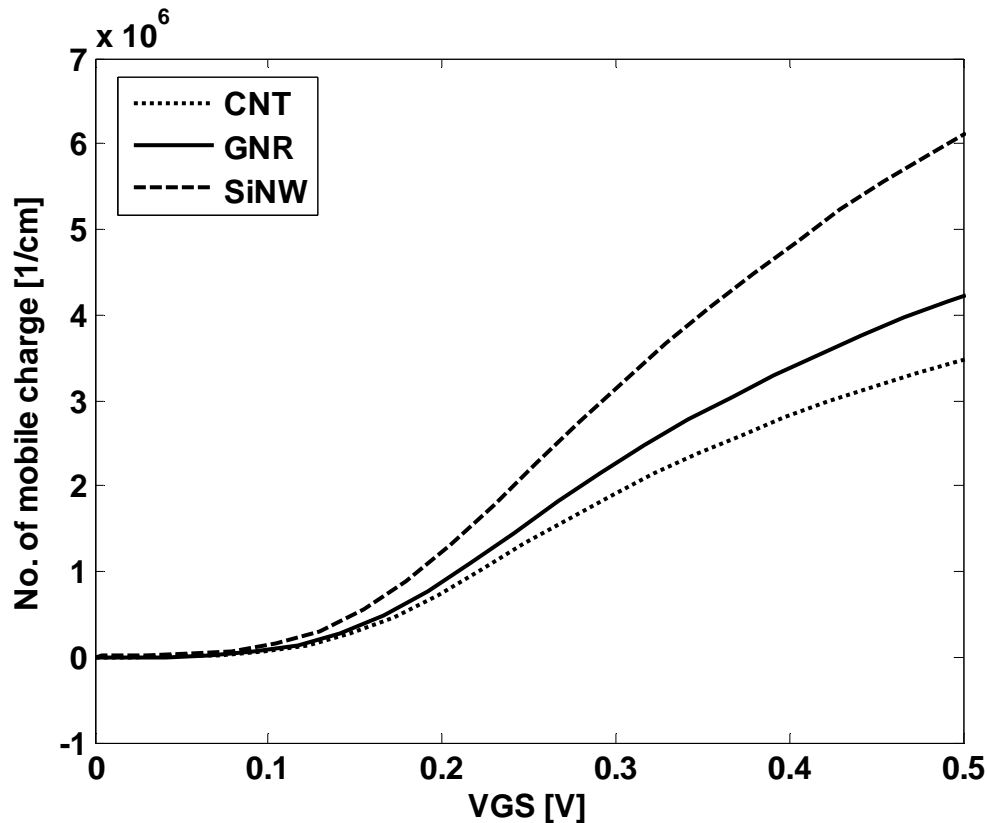

Figure 3-4: No. of mobile charge versus V_{GS} characteristics of three types of transistor at V_{DS}=0.5V

Figure 3-4 shows the number of mobile charge versus gate bias plots for a drain bias of 0.5V. In these plots, V_{GS}=0 is corresponding to a drain current of 10nA. In figure 3-4, at V_{ON} the number of mobile charge of CNT, GNR and SiNW transistors are $3.5 \times 10^6 cm^{-1}$, $4.2 \times 10^6 cm^{-1}$ and $6.1 \times 10^6 cm^{-1}$. The reason behind the better performance of GNR and CNT transistors than SiNW transistor is shown in figure 3-4. The effective mass of CNT is lighter than GNR and the effective mass of GNR is lighter than SiNW and from the eqution of density-of-states(DOS) it is known that DOS is directly propotional to the square root of effective mass of electron. Higher DOS of SiNW provides higher channel charge density.
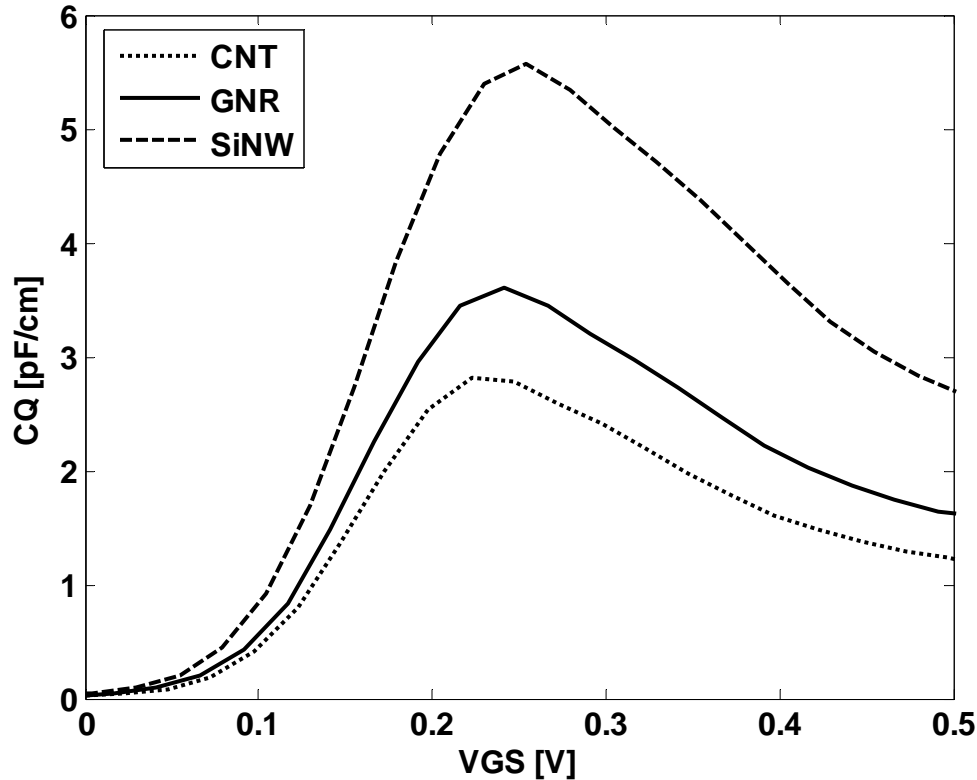
Figure 3-5: Quantum capacitance versus V_{GS} characteristics of three types of transistors at $V_{DS}=0.5V$

Figure 3-5 shows the quantum capacitance versus gate bias plots for a drain bias of 0.5V. In these plots, $V_{GS}=0$ is corresponding to a drain current of 10nA. From figure 3-5 we can observe that SiNW has higher quantum capacitance than GNR transistor. And GNR transistor has higher quantum capacitance than CNT transistor. Small quantum capacitance is an important requirement for effective gate control of transistors. The quantum capacitance is proportional to the density-of-states(DOS) at fermi energy. As CNT has the lowest DOS due to the lightest effective mass, its quantum capacitance is the least and that of SiNW is the highest. In figure 3-5, the peak value of quantum capacitance of SiNW, GNR and CNT transistors are 5.6pF/cm, 3.6pF/cm and 2.8pF/cm. Figure 3-5 shows that when V_{GS} increases from 0, energy of the top of the barrier decreases, so the top of the barrier gets close to fermi level and that's why quantum capacitance increases. This condition is valid until the energy of top of the barrier is greater than fermi energy. When fermi energy is equal to the top of the barrier energy, then the quantum capacitance reaches to its peak value. Again when top of the barrier energy is less than fermi energy and still decreases by increasing V_{GS} then quantum capacitance decreases slowly.
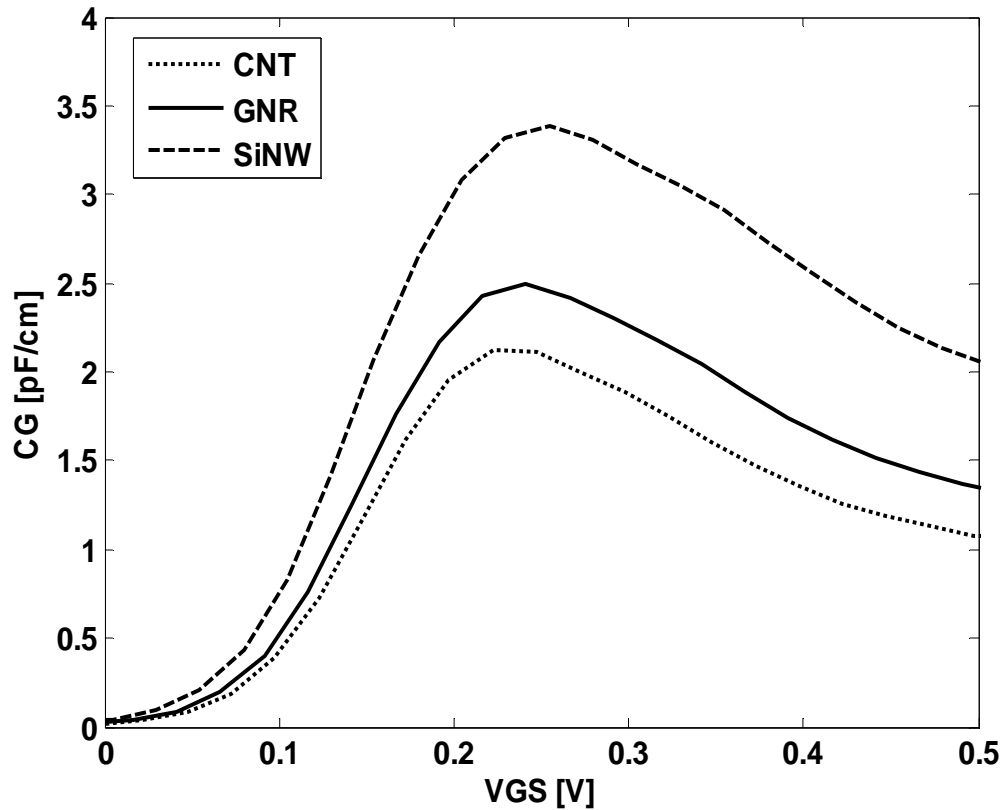
Figure 3-6: Gate capacitance versus V_{GS} characteristics of three types of transistor at V_{DS}=0.5V

From equation 2.39 C_G is calculated. Figure 3-6 shows the gate capacitance versus gate bias plots for a drain bias of 0.5V. In these plots V_{GS}=0 is corresponding to a drain current of 10nA. Here C_{OX} is constant but depends on channel material and shape. Quantum capacitance is in the series of C_{OX} and C_Q. So C_G is primarily controlled by C_Q, because of small C_Q the series combination of C_Q and C_{OX} is less than C_Q. And so by comparing figure 3-5 and figure 3-6, it is being observed that the total gate capacitance decreases almost 45% than quantum capacitance. From figure 3-6, the peak values of gate capacitance of SiNW, GNR and CNT transistors are 3.5pF/cm, 2.3pF/cm and 2pF/cm.
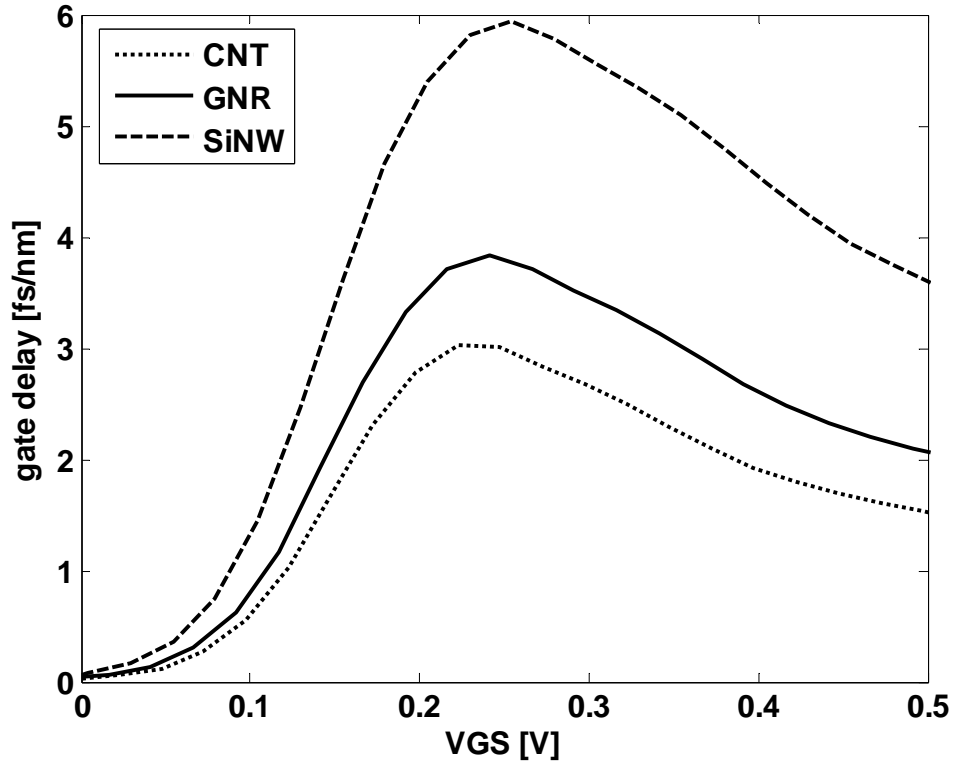
Figure 3-7: Gate delay versus V$_{GS}$ characteristics of three types of transistors at V$_{DS}$=0.5V
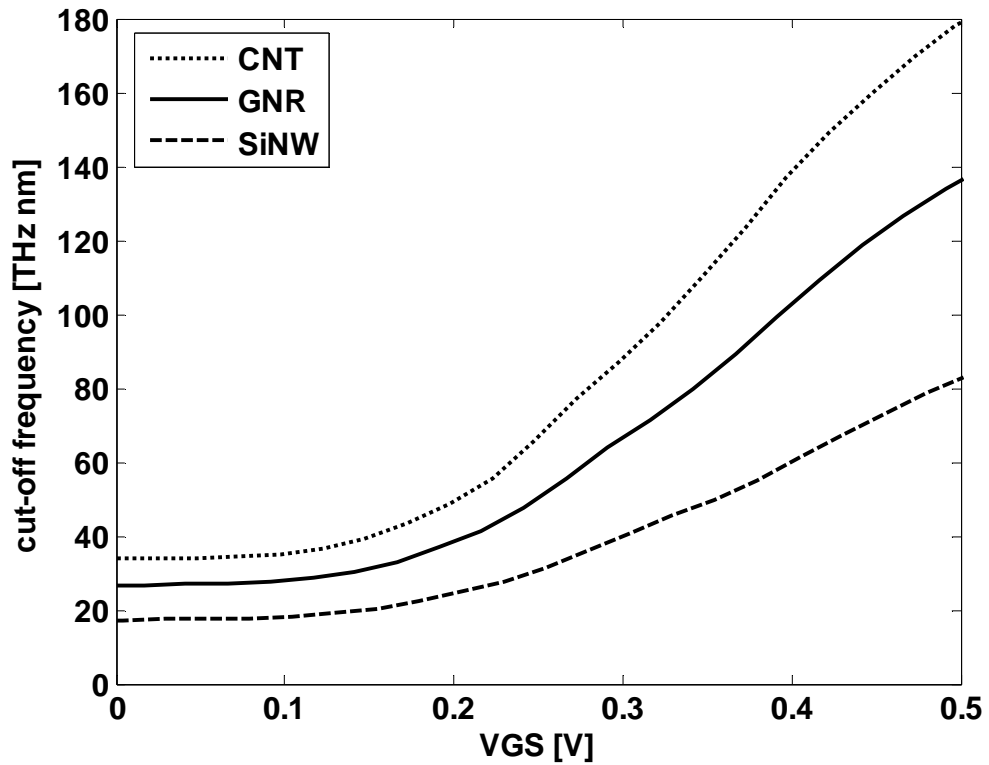

Figure 3-8: Cut-off frequency versus V$_{GS}$ characteristics of three types of transistors at V$_{DS}$=0.5V

Gate delay is calculated using equation 2.40. Figure 3-7 shows the gate delay versus gate bias plots for a drain bias of 0.5V. In these plots, $V_{GS}=0V$ is corresponding to a drain current of 10nA. As we know the lower the value of gate delay, the more effective the FET becomes as a switch. From equation 2.40 it is known that gate delay is directly proportional to the gate capacitance and inversely proportional to the on-current. On-current is individually constant for different types of transistors which are shown in figure 3-1. So to achieve low gate delay it is necessary to have high on-current and low gate capacitance. From figure 3-7, the peak values of gate delay of SiNW, GNR and CNT transistors are 5.93fs/nm, 3.83fs/nm and 3fs/nm.

Figure 3-8 shows the cut-off frequency versus gate bias plots for a drain bias of 0.5V. In these plots, $V_{GS}=0$ is corresponding to a drain current of 10nA. From equation 2.41 it is known that cut-off frequency is directly proportional to the transconductance and inversely proportional to the gate capacitance. As we know the higher the magnitude of cut-off frequency, the more effective the FET becomes as a switch. So cut-off frequency is an important performance metric for high frequency performance of a transistor. So to achieve good amplifier response from a transistor it is necessary to have high transconductance. In figure 3-8, it is shown that the cut-off frequency of CNT, GNR and SiNW transistors are 178.2THz nm, 134.1THZ nm and 83.4THz nm.

Table 3-2: Simulated values of I_{ON}, I_{ON}/I_{OFF}, g_m, C_Q, τ, and f_T of three types of transistors.

Device	CNTFET	GNRFET	SiNWFET
I_{ON} [uA]	35.14	32.61	28.53
I_{ON}/I_{OFF}	3.514×10^3	3.261×10^3	2.853×10^3
g_m [mS]	0.1207	0.1154	0.1068
C_Q(peak) [pF/cm]	2.817	3.601	5.571
τ(peak) [fs/nm]	3.023	3.831	5.935
f_T(on) [THz.nm]	178.2	134.1	83.39

4. CONCLUSION

We have studied the performance comparison of graphene and silicon nanowire transistors. We have simulated the I-V characteristics of carbon nanotube, graphene nanoribbon, and silicon nanowire transistors. Also we have seen the characteristics of transconductance, number of mobile charges, cut-off frequency, quantum capcitance and gate capacitance. For every simulation we set a common off-current 10nA. We have got better performance in CNT transistor compare to GNR and SiNW transistors. It has observed that CNT got higher on-current than GNR. And SiNW got almost lower on-current compare with GNR. So I_{ON}/I_{OFF} ratio of GNR must be higher than SiNW but lower than CNT. At on state CNT transistor shows low mobile charge compare to the SiNW transitor. CNT transistor contains small quantum capacitance compare to GNR transistor. And SiNW transistor got higher quantum capacitance than CNT transistor. For SiNW top of the barrier gets closer to the Fermi level so in this way quantum capacitance increases. And for CNT top of the barrier get away from the fermy energy so that quantum capacitance decreases slowly. We have got cut-off frequency of CNT transistor that is higher than GNR transistor. Lower gate delay exhibits faster performance in different transistors, as we have got low gate delay for GNR transistor compare to SiNW transistor and CNT transistor shows lower gate delay than GNR transistor. Considering CNT transistor is good amplifier compare to GNR and SiNW transistors by showing higher frequency performance and higher transconductance.

5. FUTURE WORK

Investigating GNRFET, CNTFET and SiNWFET characteristics are very interesting since the device has many aspects that can be explored and improved. There are various work progresses going on over these FETs like exploration over device operation, scaling issues, optimal device design etc. Our Future works will focus on add and study the tunneling effect in nano scale transistor. Then use the 2-D Poisson's equation in the process and study the effect of fringing capacitance in characteristics. Working on these areas will give us a clearer picture of their performance. The outcome of simulation analysis in this work is totally based on ideal condition; an experimental work including the fabrication process will provide us more realistic result.

6. REFERENCES

[1] Yijian Ouyang, Youngki Yoon, and Jing Guo, "Scaling Behaviors of Graphene Nanoribbon FETs: A Three Dimensional Quantum Simulation Study",IEEE Transactions on Electron Devices, Vol. 54, pp. 2223-2231, September 2007.

[2] Y. Ouyang, Y. Yoon, J. K. Fodor, and J. Guo, "Comparison of performance limits for carbon nanoribbon and carbon nanotube transistors", Applied Physics Letters, vol. 89, pp. 203107.1-203107.3, 2006.

[3] M. Lundstrom and J. Guo, "Nanoscale transistors: device physics, modeling and simulation", New York: Springer,vol. 8,pp. 224, 2006

[4] Pavel B. Sorokin, Pavel V. Avramov, Viktor A. Demin, Keonid A. Shernozatonskii, "Metallic Beta-Phase Silicon Nanowires:Structure and Electronic Properties",vol.1,13 Jun 2009.

[5]V Schmidt, J V Wittemann, U Gösele, "Growth, Thermodynamics, and Electrical Properties of Silicon Nanowires",Vol. 110, Issue: 1, Publisher: American Chemical Society, pp. 361-388,2010.

[6] B. Aradi, L. E. Ramos, P. Deák, Th. Köhler, F. Bechstedt, R. Q. Zhang, and Th. Frauenheim, "Theoretical study of the chemical gap tuning in silicon nanowires",vok. 76,issue 3,Jul 2007.

[7]Jeroen W. G. Wilder, Liesbeth C. Venema, Andrew G. Rinzler, Richard E. Smalley & Cees Dekker, "Electronic structure of atomically resolved carbon nanotubes", Nature, Vol. 391, pp. 59, Jan 1998.

[8]Leonardo de Camargo e Castro, "Modeling of Carbon Nanotube Field-Effect Transistors", The University Of British Columbia July 2006.

[9] Inauguraldissertation zur Erlangung der W¨urde eines Doktors der Philosophie vorgelegt der Philosophisch-Naturwissenschaftlichen Fakult¨at der Universit¨at Basel Von Mark Robertus Buitelaar aus Den Haag (NL), "Electron Transport in Multiwall Carbon Nanotubes", Basel, 2004.

[10] G. Liang (NUS), Neophytos Neophytou (Purdue), Mark S. Lundstrom (Purdue), Dmitri Nikonov (Intel) , "Theoretical study of graphene nanoribbon field-effect transistors", 887.016 (Purdue University), Vol. 1,pp-127 − 130, Nanotech 2007.

[11]Mceuen, P.L. Lab. Of Atomic & Solid State Phys.,Cornell Univ., Ithaca, NY Fuhrer, M.S. ; Hongkun Park, "Single-Walled Carbon Nanotube Electronics",Vol. 1,Issue: 1, pp. 78-85, Mar 2002.

[12] Martel, R.; Schmidt, T.; Shea, H. R.; Hertel, T.; Avouris, Ph., "Single and Multi-wall Carbon Nanotube Field-Effect Transistors",Vol. 73,Issue:17, pp. 2447-2449, Oct 1998

[13] Biao Kan**,** Jianning Ding**,** Ningyi Yuan**,** Junxiong Wang**,** Zhigang Chen and Xiaoshuang Chen, "Transverse electric field–induced deformation of armchair single-walled carbon nanotube",Vol. 5,Issue 7,May 2010.

[14] Oded Hod and Gustavo E. Scuseria, "Half-Metallic Zigzag Carbon Nanotube Dots",ACS Nano, Vol. 2,Issue 11, pp. 2243-2249, 2008,

[15] Max C. Lemme, "Current Status of Graphene Transistors", Solid State Phenomena Vol. 156-158,pp. 499-509, (2010).

[16] G. Fiori, G. Iannaccone, "Simulation Graphene of Nannoribbon Field Effect Transistors", IEEE Electron Device Letters, Vol. 28, Issue 8, pp. 760 - 762, 2007.

[17] A.V. Rozhkov, G. Giavaras,Yury P. Bliokh, Valentin Freilikher, and Franco Nori, "Electronic properties of mesoscopic graphene structures: charge confinement and control of spin and charge transport", Phys. Rep. 503 pp. 77-114 (2011).

[18] Gengchiau Liang Sch. of Electr. & Comput. Eng., Purdue Univ., West Lafayette, IN Neophytou, N. ; Nikonov, D.E. ; Lundstrom, M.S., "Performance Projections for Ballistic Graphene Nanoribbon Field-Effect Transistors", Vol.54 , Issue: 4 ,pp. 677 – 682, April 2007.

[19] A. K. Geim and K. S. Novoselov, "The rise of graphene,Nature Materials", vol. 6, pp. 183–191, 2007.

[20]Ricardo Faccio, Pablo A Denis, Helena Pardo,Cecilia Goyenola ,and A lvaro WMombru, "Mechanical properties of graphene nanoribbons",J. Phys.: Condens.Matter, vol. 21, pp. 285304-285311, 2009.