Sensitivity Tuning of Si Nanowires Through Backgate Bias Arrangement for Biosensing Application

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Declaration

We, hereby certify that our thesis work solely to be our own scholarly work. To the best of our knowledge, it has not been shared from any source without the due acknowledgement and permission. It is being submitted in partial fulfillment of requirements for the degree of Bachelor of Science in Electrical and Electronics Engineering. It has been submitted before any degree or examination of any other university.

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Abstract

We perform a feasibility study of tailoring sensitivity of Si nanowire through backgate bias arrangement for Biosensing application. A 100nm thick and 1µm nanowire with doping concentration of 10^{16} cm^{-3} is investigated for different backgate voltages. It is found that backgate bias has significant effect on the sensitivity of p-type Si-NW. Backgate bias for depletion of NW body is found to increase sensitivity of NWs whereas backgate bias for significant carrier accumulation is found to decreases sensitivity of NW. Sensitivity trend of NWs also found to depend on the polarity of drain voltages. When drain voltage is positive, presence of DIBL on the sub-threshold characteristics is found to shift sensitivity curve towards positive top gate voltage with increasing drain voltages. Presence of DIBL on sub-threshold characteristics is somehow found to beneficiary for biosensing application as it provides maximum sensitive operation of Si-NW even without any liquid gating of the top gate. Considering current detection capacities of semiconductor parameter analyzer available in the market a positive drain voltage of 0.9V is found to provide a maximum sensitivity of 2×10^{3}%/V even without any liquid gating. Simulation also shows that it is possible to get NWs sensitivity greater than 2×10^{3}%/V using liquid gating and providing drain voltages less than 0.5V. When drain voltage is negative no DIBL is observed in the sub-threshold characteristic which mandates liquid gating of the top gate for maximum sensitive operation of Si-NW as biosensor. These results are very significant of p-type Si-NW based biosensors fabricated on SOI platform to ensure maximum sensitive operation for molecular level detection.

Acknowledgment

It is with immense gratitude that we acknowledge the help and help of our supervisor, Dr. Mohammad Mojammel AL Hakim, Associate Professor of Department of Electrical and Electronics Engineering, East West University. Without his guidance, encouragement and support this thesis would have remained a dream. We consider it an honor to work with him. We also indebted to our parents, other professors of the department, and friends for their support and encouragements. Finally thanks to almighty who gave us the patience to finish the task successfully.

Authorization Page

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CHAPTER 1: INTRODUCTION

1.1 Motivation and Objective

Over the past daces semiconductor nanowires are materials of great interest due to their unique electrical characteristics for biochemical sensors applications. Biosensors based on silicon nanowire field-effect transistors (Si-NW-FETs) have drawn huge amounts of attention, due to their ultra sensitivity, label-free and real-time detection abilities. This ultra-high sensitivity detection can be attributed to their smaller size and large surface to volume ratio, enabling local charge transfers to result in a current change due to a field effect when analytic molecules bind to a specific recognition molecule at the surface of the nanowire[1]. The effect is so strong that signal charge at the surface of the nanowire can even deplete or accumulate the entire cross sectional conductor path of these nanostructures [2].

Plenty of works can be found in the literature employing Si-NWs for detecting biomarkers, individual bacteria or viruses. Unfortunately, in most of these works Si-NWs inherent characteristics have not been considered in detailed in which could have provided much better and unambiguous detection of biomarkers, bacteria or viruses. Si-NWs are traditionally formed on SOI wafers using top down approaches and its buried Si layer could easily be used as an additional gate which may affect Si-NWs sensitivity as biosensor. In this work we first time perform a systematic study on the effect of backgate bias on the sensitivity of P-Type Si-NWs. A 100 nm thick, 1µm long P-Type Si-NW with a nominal doping of 10^{16}/cm^3 has been investigated for different backgate biases and different drain bias polarities to gain insight into NW's sensitivity through backgate bias arrangements.

1.2 Background

The conductance changes of silicon nanowires upon attachment of bimolecular have been employed extensively for bio sensing applications. Quite a number of works [3-6] can be founded in the literature exploiting this behavior for biosensors. However inherent nanowires electrical characteristics are found to be quite variable although they have been successfully applied for bio sensing application. These are discussed below.

A typical nanowire biosensor can be a single or an array of nanowires which is laid on an insulator between source and drain [Figure. 2.1]. Electrodes of these source and drain are isolated by a protection layer. On Si-NW surface, target receptors which have the capability of immobilizing the targets, e.g. ions, DNA, proteins are attached by molecular linkers. Due to large surface to volume ratio, the charges associated with the attached molecules can be deplete or accumulate entire cross sectional pathway. And hence nanowire conductance gets easily changed. This phenomenon resulted in the most promising breakthrough in the 21st century by

possible application of simple nanowire device for disease diagnosis [7-11, 12-14].
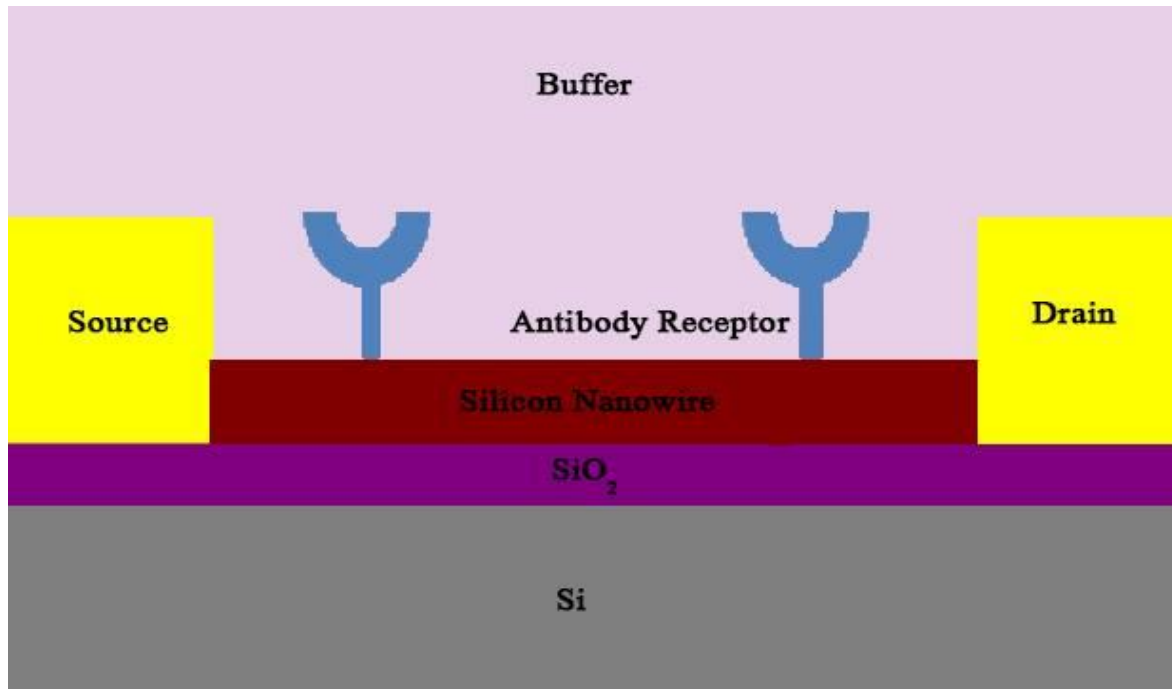

Figure 1.1: Schematic diagram of the structure of Si-NW biosensor.

Lieber et al. [3] successfully fabricated silicon nanowire biosensors on p-type semiconductor where the typical DC current voltage (I-V) characteristics were linear. The ability of the fabricated biosensors was tested through pH response with or without modifying nanowire surface containing both amino or silanol receptor. It was shown that increase of the solution pH level resulted in the increase of nanowire conductance due to the reduction of the protons in the solution and vice versa with typical sensitivity around 10% to 20% only. Real time detection of clinically relevant protein streptavidin was demonstrated down to concentrations of 10pM. Single DNA and wild type virus the DF508 also detected. This electrical detection was done to concentration of 60fM. These results exhibited the promise of silicon nanowires as biosensor where nanowire's inherent DC characteristics were linear demonstrated general concept of nanowires just as simple constricted dimension resistors.

Chen et al. [15] fabricated p-type silicon nanowires using anew size reduction method where silicon nanowires have height of 140nm, width of 100nm with triangular structure and a uniform doping concentration of $N_a=10^{17}$ cm^{-3}. Measured current voltage (I-V) characteristics exhibited typically non-linear diode like characteristics. According to provided I-V curves there were no conduction up to a drain bias of $V_{ds}<1V$. The conduction of nanowires were improved through the application of negative back gate bias thereby increasing the accumulation of holes and at

$V_{backgate}$ = -20Vthe I-V characteristics showed linear behavior. It was noticeable that at small negative $V_{backgate}$ I-V characteristics were typically nonlinear. This was attributed to the fixed electronic charge located in the front oxide near the top silicon device layer surface and buried oxide near the bottom of silicon device layer due to reactive thermal oxidation of silicon surface. These nanowires were also successfully sensed pH level of the solution with sensitivity around 40mV/pH
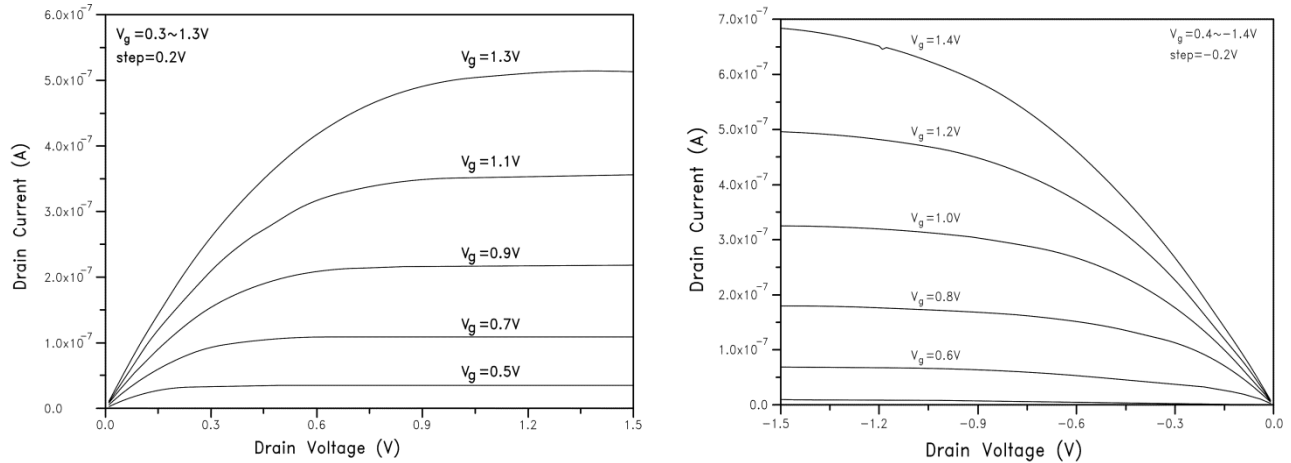
Figure 1.2: Measured output characteristics of junction less accumulation mode silicon nanowire transistors; a) drain current versus drain voltage for an n-type silicon nanowire and b) drain current versus drain voltage for different values for gate voltages for a p-type silicon nanowire. The width, W is 20nm and the gate length, L, is 1µm, such that W/L = 0.02 (courtesy Jean-Pierre Colinge et al. [16].

Most recently, Jean-Pierre Colinge et al. [16] first time reported that Si-NWs with a a few tens of nanometers wide, thickness of 20nm and uniform doping concentrations around $10^{19}cm^{-3}$, behave as transistor than simple resistor. Both p-type and n-type silicon nanowires were fabricated and measured characteristics showed that both n-type and p-type devices exhibited transistor action. These devices showed near ideal sub-threshold slope of 64mv dec^{-1} and quite decent output characteristics. Figure 1.2 and 1.3 shows that measured sub-threshold and output characteristics of such accumulation mode silicon nanowire transistors.

The aforementioned analysis shows quite a variable DC characteristic of Si-NWs and application as biosensor without adequate justification resulting in random application of biases. This resulted excellent sensitivity of SiNW somehow unexploited.
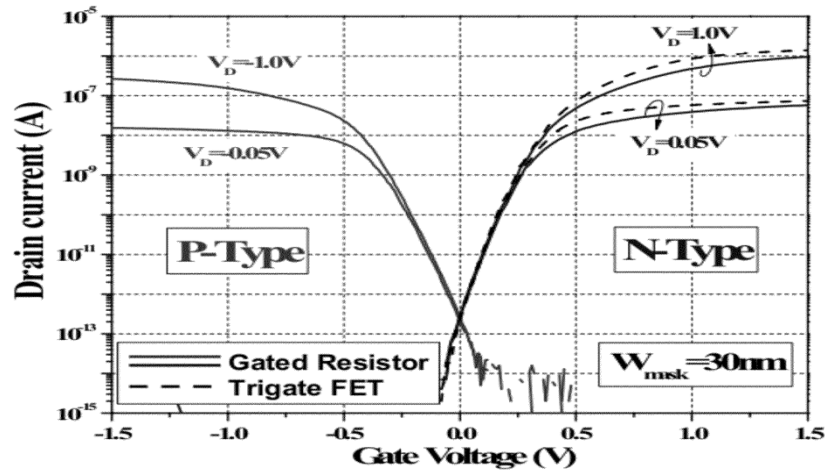
Figure 1.3: Measured sub-threshold characteristics of junction less accumulation mode silicon nanowire transistors. Drain current versus gate voltage for drain voltage of ±50mV and ±1 V for n-type and p-type silicon nanowires. The width of the nanowires is 30nm and the gate length, L, is 1μm (courtesy: Jean-Pierre Colinge et al. [15])

1.3 Organization

Chapter 1 provides the necessary background work on the electrical Characteristics of silicon nanowires. A number of research papers on Si-NW biosensor have also been surveyed to gain an understanding on the importance of this work.

Chapter 2 Describe device structures, simulation mythology and the required models for the simulation.

Chapter 3 Describe the simulation results for nanowire thickness of 100 nm with doping density 10^{16} cm^{-3} for different backgate bias condition.

Finally, in chapter 4 and in chapter 5, the contribution of this work is summarized and discussed.

CHAPTER 2: METHODOLOGY

2.1 Device features and simulation models

The investigation on the sensitivity of Silicon nanowire for biosensor application were done with the help of numerical simulations using the SILVACO Atlas device simulator [17], installed on a VLSI lab of East West University. A p-type silicon nanowire with 100nm thickness was created on 100 nm oxide with a 500 nm buried Si layer. A secondary gate (backgate) is made with 20nm Al beneath the buried Si layer. The gate oxide thickness was 2nm and a heavily doped poly-silicon layer was used as top gate material. In the silicon nanowire, two heavily doped regions on the two sides of the channel were employed to ensure ohmic contacts on the source/drain regions. The gate doping was 10^{20}/cm^3 and the source/drain regions were also heavily doped with the doping density of 10^{20}/cm^3. The channel doping was 10^{16}/cm^3. Here, the gate doping was n-type whereas the drain and the channel doping was p-type. To contact source to drain and gate, aluminum electrode was chosen.
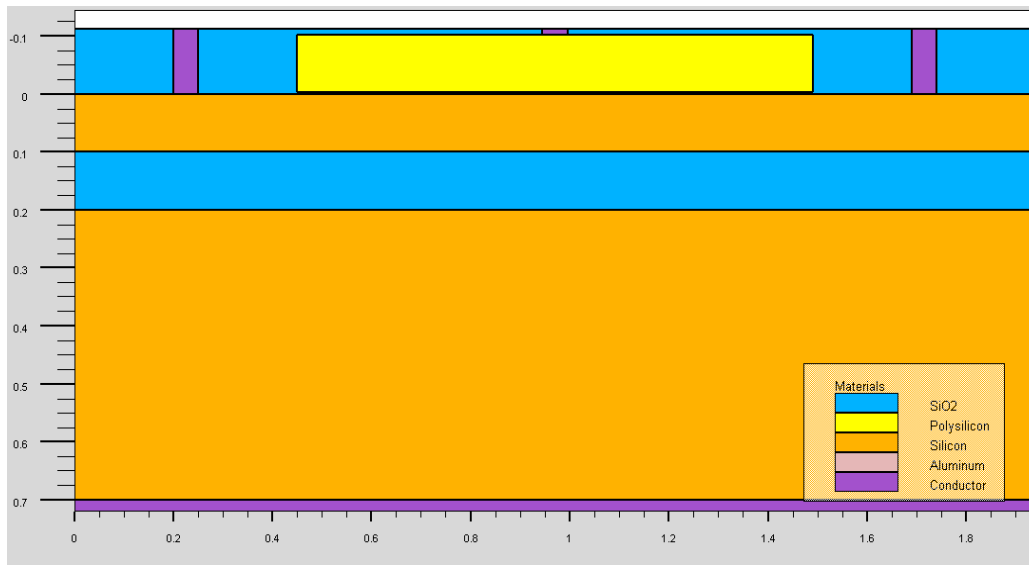
Figure 2.1: Schematic of the simulated p-type silicon nanowire.

As Si-NW is 100nm thick quantum effect is neglected and a classical drift diffusion model is used to investigate Si-NW behavior. To accurately model carrier mobility in the constricted volume of NW Lombardi (CVT) model was used to take account temperature (T_L), perpendicular electric field ($E\perp$), parallel electric field ($E\parallel$) and doping concentration (N) effects [15]. In the CVT model, the transverse field, doping dependent and temperature dependent parts of the mobility are given by the three components that are combined using Mathiessen's rule. These components are surface mobility limited by scattering with acoustic phonons (μ_{AC}), the

mobility limited by surface roughness (μ_{sr}) and the mobility limited by scattering with optical intervalley phonons (μ_b) are combined using Mathiessen's rule as follows [17]:

$$\mu_T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{sr}^{-1} \tag{2.1}$$

The first component, surface mobility limited by scattering with acoustic phonons equations [17]:

$$\mu_{AC.n} = \frac{BN.CVT}{E_\perp} + \frac{CN.CVT \ N^{\tau.CVT}}{T_L \ E_\perp^{1/3}} \tag{2.2}$$

$$\mu_{AC.p} = \frac{BN.CVT}{E_\perp} + \frac{CP.CVT \ N^{\tau P.CVT}}{T_L \ E_\perp^{1/3}} \tag{2.3}$$

The equation parameters BN.CVT, BP.CVT, CN.CVT, CP.CVT, TAUN.CVT, and TAUP.CVT used for this simulation are shown in Table 3-1 [18].

The second component, μ_{sr} is the surface roughness factor and is given by [17]:

$$\mu_{sr} = \frac{DELN.CVT}{E_\perp^2} \tag{2.4}$$

$$\mu_{sr} = \frac{DELP.CVT}{E_\perp^2} \tag{2.5}$$

The equation parameters DELN.CVT and DELP.CVT used for this simulation are shown in Table 3.1[17].

The third mobility component, the mobility limited by scattering with optical intervalley phonons is given by [17]:

$$\mu_{b,n} = MU0N.CVT exp\left(\frac{-PCN.CVT}{N}\right) + \frac{\left[MUMAXN.CVT \left(\frac{T_L}{300}\right)^{-GAMN.CVT} - MU0N.CVT\right]}{1 + \left(\frac{N}{CRN.CVT}\right)^{ALPHN.CVT}} -$$

$$\frac{MU1N.CVT}{1 + \left(\frac{CSN.CVT}{N}\right)^{BETAN.CVT}}$$
(2.6)

$$\mu_{b,p} = MU0P.CVT exp\left(\frac{-PCP.CVT}{N}\right) + \frac{\left[MUMAXP.CVT \left(\frac{T_L}{300}\right)^{-GAMP.CVT} - MU0P.CVT\right]}{1 + \left(\frac{N}{CRP.CVT}\right)^{ALPHP.CVT}} -$$

$$\frac{MU1P.CVT}{1 + \left(\frac{CSP.CVT}{N}\right)^{BETAP.CVT}} \qquad (2.7)$$

Table 2.1: Parameters for Equations 2.1 to 2.7

Statement	Parameter	Default	Units
MOBILITY	BN.CVT	4.75×10^7	cm/(a)
MOBILITY	BP.CVT	9.925×10^4	cm/(a)
MOBILITY	CN.CVT	1.74×10^5	
MOBILITY	CP.CVT	8.842×10^5	
MOBILITY	TAUN.CVT	0.125	
MOBILITY	TAUP.CVT	0.0317	
MOBILITY	GAMN.CVT	2.5	
MOBILITY	GAMP.CVT	2.2	
MOBILITY	MU0N.CVT	52.2	$cm^2/(v\text{-}a)$
MOBILITY	MU0P.CVT	44.9	$cm^2/(v\text{-}a)$
MOBILITY	MU1N.CVT	43.4	$cm^2/(v\text{-}a)$
MOBILITY	MU1P.CVT	29.0	$cm^2/(v\text{-}a)$
MOBILITY	MUMAXN.CVT	1417.0	$cm^2/(v\text{-}a)$
MOBILITY	MUMAXP.CVT	470.5	$cm^2/(v\text{-}a)$
MOBILITY	CRN.CVT	9.68×10^{14}	cm^{-3}
MOBILITY	CRP.CVT	2.23×10^{17}	cm^{-3}
MOBILITY	CSN.CVT	3.43×10^{20}	cm^{-3}
MOBILITY	CSP.CVT	6.10×10^{20}	cm^{-3}
MOBILITY	ALPHN.CVT	0.680	
MOBILITY	ALPHP.CVT	0.71	
MOBILITY	BETAN.CVT	2.00	
MOBILITY	BETAP.CVT	2.00	
MOBILITY	PCN.CVT	0.0	cm^{-3}
MOBILITY	PCP.CVT	0.23×10^{16}	cm^{-3}
MOBILITY	DELN.CVT	5.82×10^{14}	v/s

The model for carrier emission and absorption processes proposed by Shockley-Read-Hall (SRH) is used to reflect the recombination phenomenon within the device. The electron and hole lifetimes $\tau_{n\ and}\ \tau_p$were modeled as concentration dependent. The equation is given by [17]:

$$R_{SRH} = \frac{pn - n_{ie}^2}{\tau_p\left[n + n_{ie}\exp\left(\frac{ETRAP}{kT_L}\right)\right] + \tau_n\left[p + n_{ie}\,exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \tag{2.8}$$

$$\tau_n = \frac{TAUNO}{1 + \frac{N}{(NSRHN)}} \tag{2.9}$$

$$\tau_p = \frac{TAUPO}{1 + \frac{N}{(NSRHP)}} \tag{2.10}$$

Here N is called the local (total) impurity concentration. The used parameters TAUN0, TAUP0, NSRHN and NSRHP are Table 3-2[17]. This model was activated with the CONSRH parameter of the MODELS statement.

Table 2.2: Default Parameters for Equations 2.8 to 2.10

Statement	Parameter	Default	Units
METERIAL	TAUNO	1.0×10^{-7}	S
METERIAL	NSRHN	5.0×10^{16}	cm^{-3}
METERIAL	TAUPO	1.0×10^{-7}	S
METERIAL	NSRHP	5.0×10^{16}	cm^{-3}

To account bandgap narrowing effects, BGN model was used. These effects may be described by an analytic expression relating the variation in bandgap,ΔE_g,to the doping concentration,N. The expression used in ATLAS is from Slotboom and de Graaf [17]:

The used values for the parameters BGN.E, BGN.N and BGN.C are shown in Table 2.3[17].

Table 2.3: Default parameters of Slotbooms Bandgap Narrowing Model foe equation 2.11

Statement	Parameter	Default	Units
METERIAL	BGN.E	9.0×10^{16}	V
METERIAL	BGN.N	1.0×10^{16}	cm^{-3}
METERIAL	BGN.C	0.5	-

2.2 Simulation profile

Device simulation using silvaco atlas usually faces convergence problems and necessitates a long run times. To avoid these problems, the simulation of silicon nanowire MOSFET has been divided into a few groups. At first, structure definition was performed. In this definition the simulation focused on creating the structure with a suitable mesh density. Regions and electrodes were defined as depicted in figure 2.2. Finer nodes were assigned in critical areas, such as across the gate oxide for an accurate 10nm thickness to monitor channel activity and to get a better picture of the depletion layer and junction behavior near the source/drain boundaries. A coarser mesh was used elsewhere in order to reduce simulation run time.
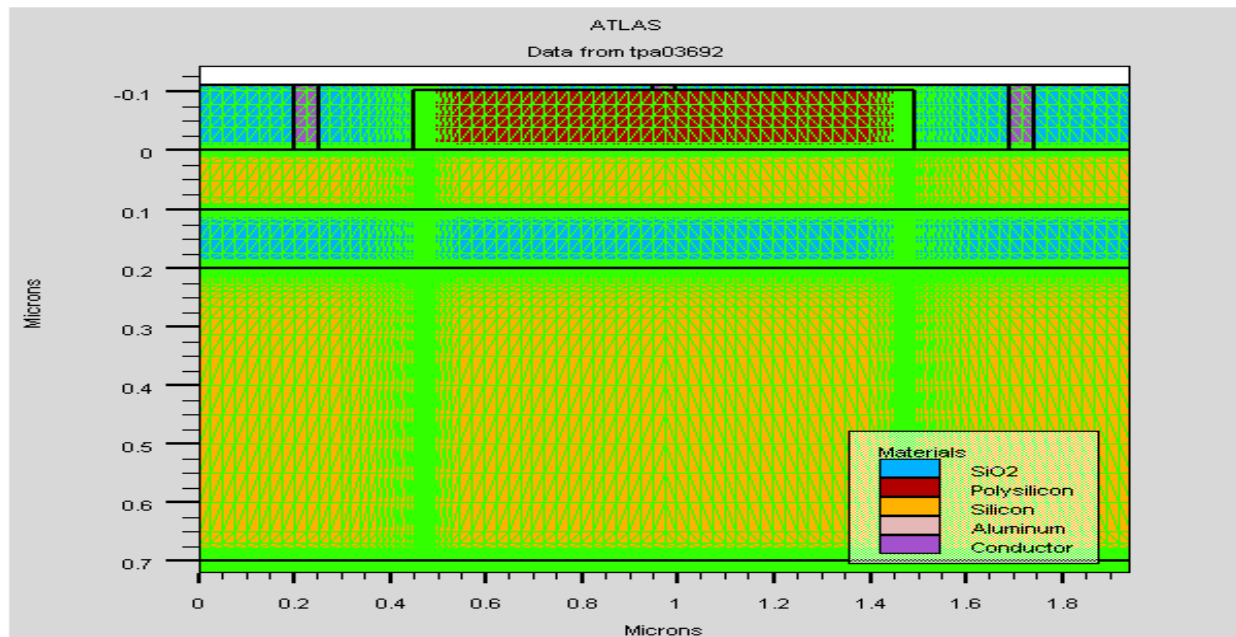
Figure 2.2: Cross-sectional view of p-type nanowire showing the mesh density used in this simulation.

Once the structure and the mesh were found to be as desired, the simulation was performed with appropriate models as discussed in section 2.1 and numerical solving methods. The model was invoked by using the statements FERMI, CVT, CONSRH, BGN. The numerical solving methods GUMMEL, NEWTON were used to reduce the simulation run time, while keeping the accuracy of the simulation at an acceptable level.

To get convergence, a special bias point solving method was used. It was found that the simulation faced difficulty in solving the initial desired bias points. i.e. ±1V, -2V, ±3V, ±4V, ±5V for backgate voltage and ±1V for drain voltage. Therefore, the initial gate bias was set to 0.005V and the next bias point was set to 0.05V, before finally setting the bias point to desired value.
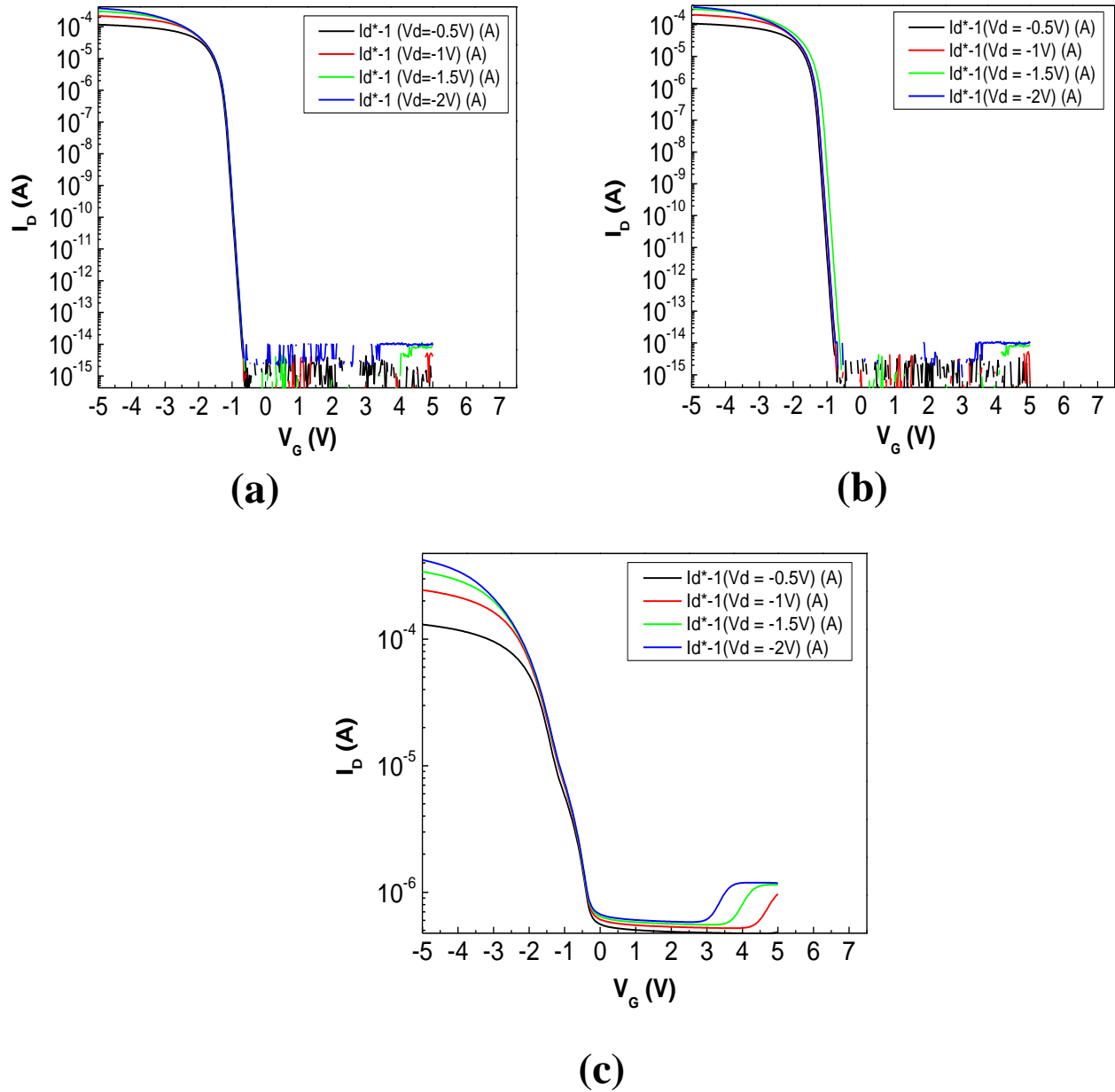
CHAPTER 3: RESULTS

(a)

(b)

(c)
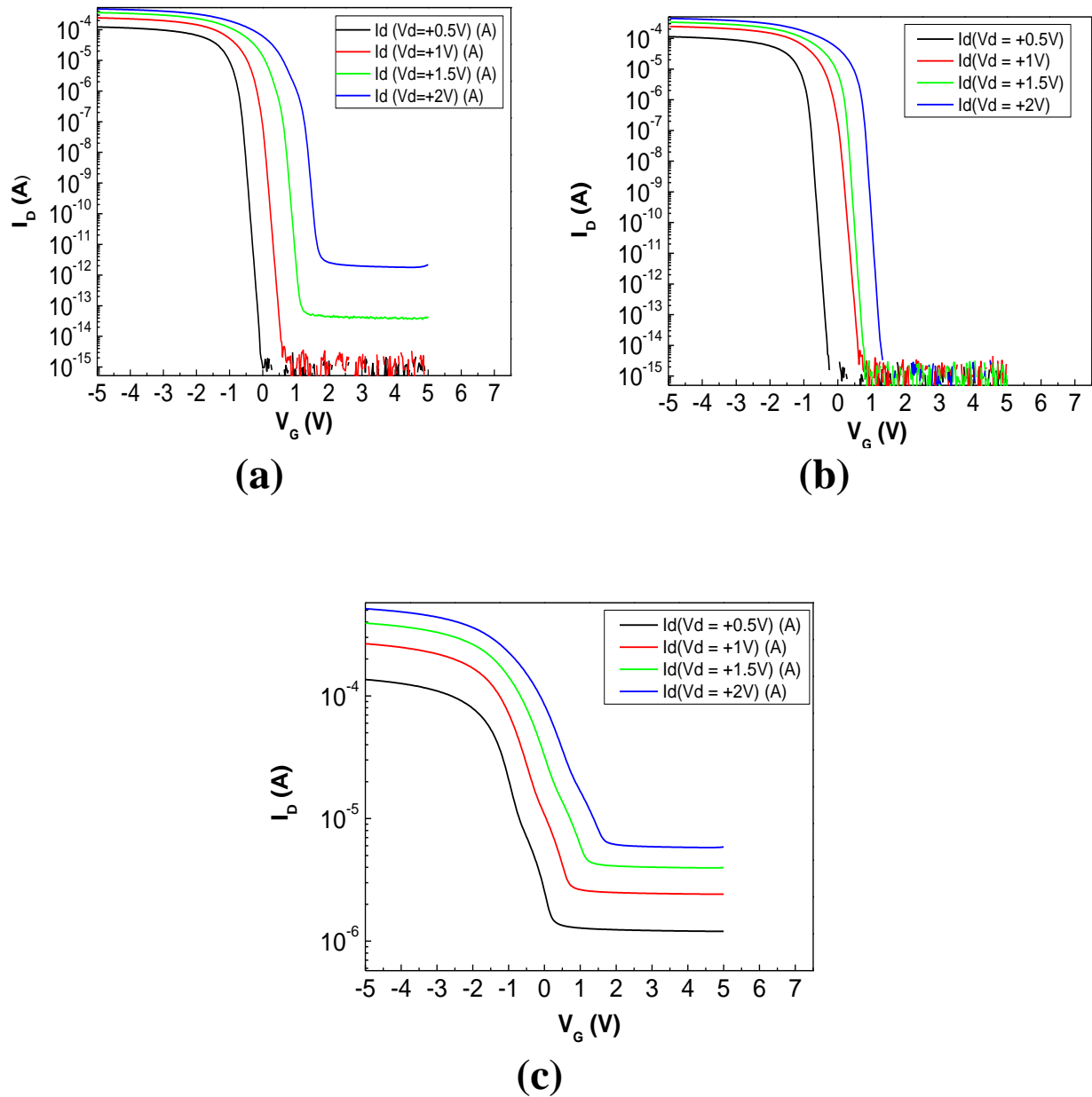
Figure 3.1 Shows transfer characteristics (I_D vs V_G) of Si-NW when V_D is positive and V_G is swiped from +5V to -5V for (a) $V_{backgate} = 0V$, (b) $V_{backgate} = +4V$ (c) $V_{backgate} = -4V$.

Figure 3.1(a to c) shows transfer characteristics (I_D vs V_G) of Si-NW when V_D is positive and V_G is swiped from +5V to -5V and for different values of backgate bias. The nanowire have thickness of 100 nm, doping concentration of 10^{16} cm^{-3} and channel length of 1μm. For backgate

bias of 0V in figure 3.1(a), it is found that the NWs exhibit quite a good transistor with a sub threshold slope of 74.6 mV/dec and DIBL is about 1100 mV/V. A sub threshold slope of 74.6 mV/dec is quite good for sensing operation as NWs can be set to exhibit excellent sensitivity with an appropriate V_G range if it can be ensured that NWs fall within the sub-threshold region of operation. However, with increasing V_D values NWs sub-threshold region shifts toward positive V_G values. This result is quite significant sensing operation as it provides liquid gating of the top-gate at different positive V_D values to get the NWs in the middle of sub-threshold region to ensure maximum sensitive operation. It is worth mentioning that liquid gating is complicated which requires costly probes and careful solution delivery on the top gate with extreme precaution is avoid shorts in device. However, figure 3.1(a) also shows that if no liquid gating is used, it is advisable to use $V_D \approx 0.9V$ to ensure NWs operating point in the middle of the sub-threshold slope for 1μm long NWs with $V_{backgate} = 0V$.

Figure 3.1(b) shows the transfer characteristics (I_D vs V_G) of Si-NW when V_D is positive and V_G is swapped from +5V to -5V and backgate voltage are +4V. For back gate voltage of +4V again it is found that the NWs exhibit a good transistor with a sub threshold slope of 67.7mV/dec and DIBL is about 1000 mV/V which is similar to that of the 0V backgate bias. This result is imply that for p-type NW depletion of NW body by back gate beyond carrier level of $10^{16}/cm^3$ does not degrade device performance as a sensor. Sensor performance remains similar to that of the $V_{backgate}=0V$.

To further characterize the NW behavior, figure 3.1(c) shows the transfer characteristics (I_D vs V_G) of silicon NW when V_D is positive and V_G is swapped from +5V to -5V and for backgate voltage of -4V. The nanowire have thickness of 100 nm, doping concentration of 10^{16} cm^{-3} and channel length of 1μm. It is found that the NWs exhibit quite a degraded transistor behavior with a sub threshold slope of 108.2 mV/dec and DIBL is 1000 mV/V. As sub-threshold region of operation ensures maximum sensitivity of NW based sensor this result imply that accumulation of carriers in p-type NW by backgate control actually degrades device performance as sensor. However, figure 3.1(a to c) show that NWs sensitivity can be easily adjusted through backgate control which actually provides flexibility of NW based biosensor in SOI wafer based platform.

Figure 3.2(a to c) shows the transfer characteristics (I_D vs V_G) of Si-NWs when V_D is negative and V_G is swapped from +5V to -5V and for different values of backgate bias. The nanowire have thickness of 100 nm, doping concentration of 10^{16} cm^{-3} and channel length of 1μm. For back gate of 0V figure 3.2(a) NWs exhibit an excellent transistor behavior with sub threshold slope of 66.8 mV/dec and interestingly there is no DIBL. There is no shift of I_D vs V_G curves with V_D values up to -2V. In contrast to positive V_D applications (fig 3.1), negative V_D although exhibits
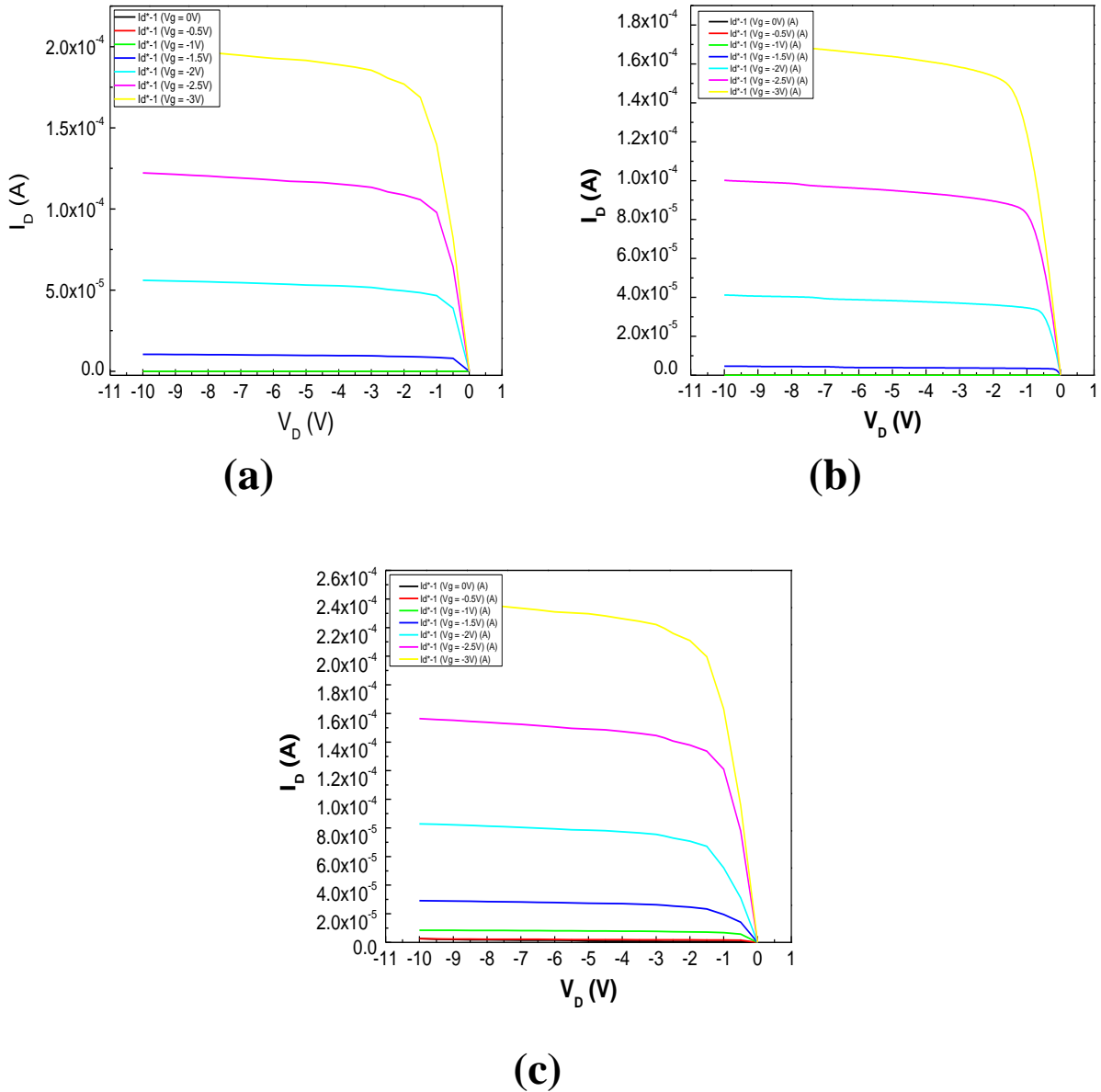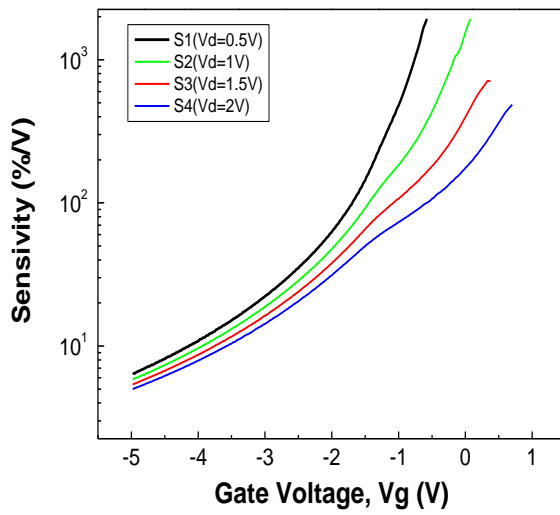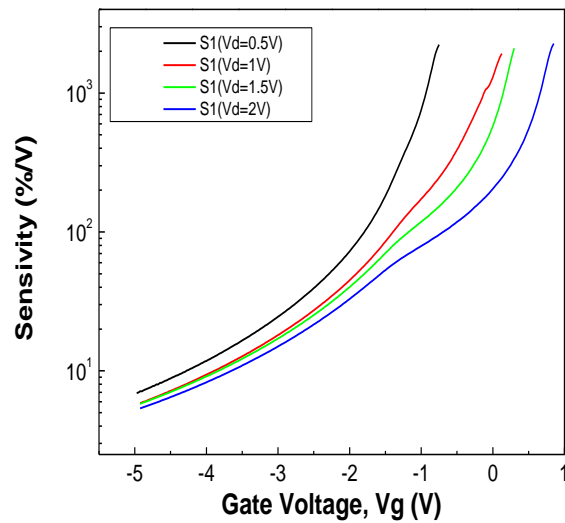
Figure 3.2 Shows transfer characteristics (I_D vs V_G) of Si-NW when V_D is negative and V_G is swiped from +5V to -5V for (a) $V_{backgate} = 0V$, (b) $V_{backgate} = +4V$ (c) $V_{backgate} = -4V$.

better transistor behavior it somehow make it imperative to apply liquid gating to set NWs at the middle of sub-threshold region for sensitive operation of NWs as biosensor. For $V_{backgate}=+4V$ at, sub-threshold slope with 67.8 mV/dec does not change too much from the case when $V_{backgate}$ was 0V, implying similar sensor operation for both $V_{backgate}=0V$ and +4V. For $V_{backgate}=-4V$ in figure 3.2(c), degradation of sub-threshold characteristics with a value 110mV/dec can be observed but there is no degradation in DIBL characteristics. As, DIBL non significant effect on the sensitivity of NWs, it can be concluded that when V_D is negative, sensor application is similarly degraded to that of V_D positive, if too much carrier accumulation happens in NW.
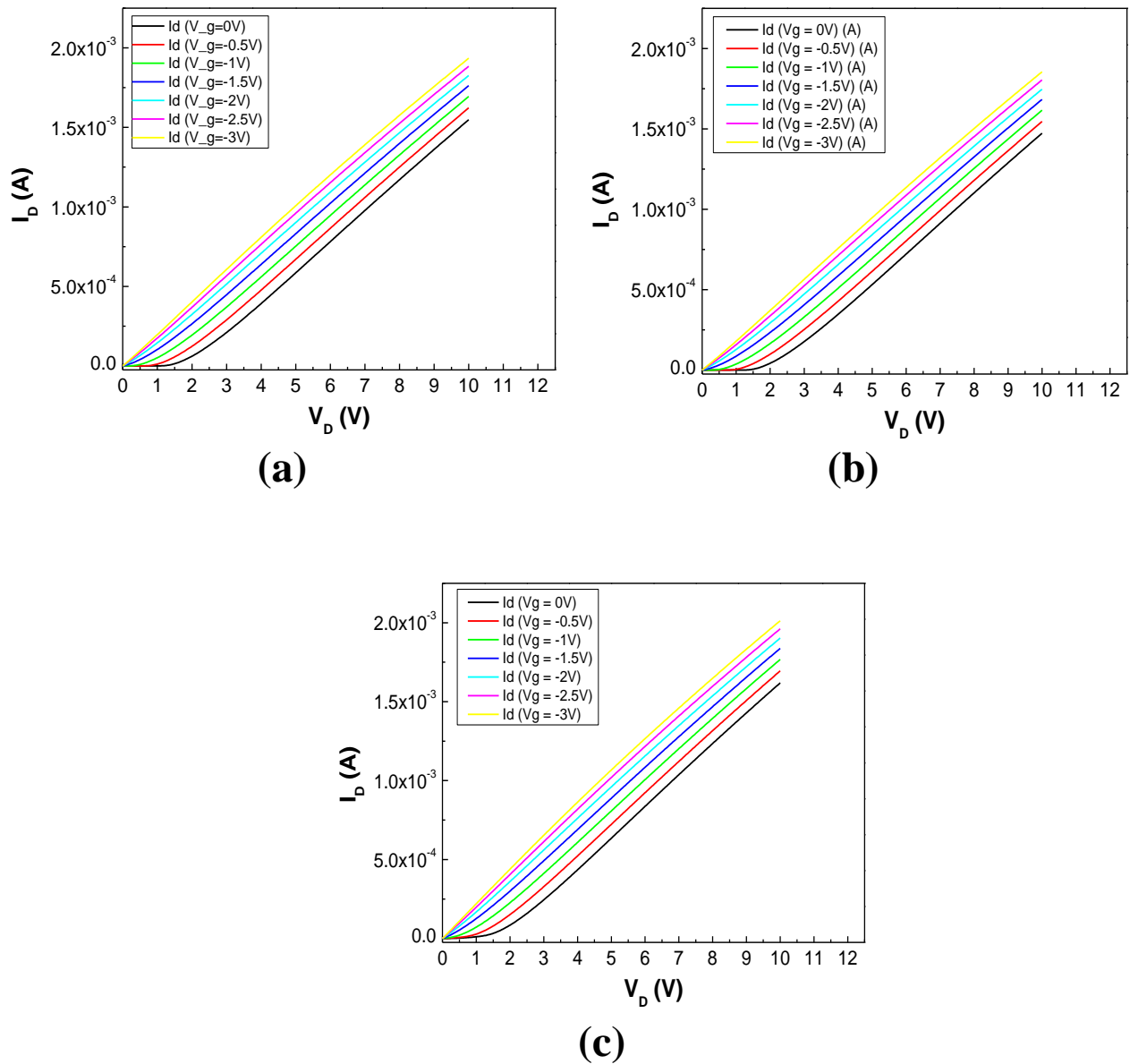
Figure 3.3 Shows output characteristics (I_D vs V_D) of Si-NW when V_D is positive and V_G is swiped from +5V to -5V for (a) $V_{backgate} = 0V$, (b) $V_{backgate} = +4V$ (c) $V_{backgate} = -4V$.

Figure 3.3(a to c) shows the I_D-V_D characteristics, when the drain voltage is positive for different backgate voltages. The nanowire have thickness of 100 nm, doping concentration of $10^{16}cm^{-3}$ and channel length of 1µm. For backgate of 0V (fig 3.3(a)) it is found that I_D vs V_D characteristics are non linear when V_G=0V and there is no conduction up to certain level of V_D. With negative V_G values it can be seen that I_D increase and trend gradually becomes linear.

For $V_{backgate}$ of +4V similar characteristics are observed. However, the drain voltages up to which no conduction can be seen to increase for V_G=0V. The I_D values also decrease when $V_{backgate}$=+4V in comparison to figure 3.3(a) when $V_{backgate}$ was 0V. Significant depletion of channel region of p-type NWs for $V_{backgate}$=+4V can be attributed to this.

For $V_{backgate}$=-4V, I_D increases in comparison to $V_{backgate}$=0 and +4V and the V_D values up to which there is no conduction decreases. However, for positive V_D application (fig 3.3 a to c) although sub-threshold characteristics show transistor like behavior I_D-V_D characteristics does not saturate. It rather shows linear gated resistor like behavior.

(a)

(b)

(c)

Figure 3.4 Shows output characteristics (I_D vs V_D) of Si-NW when V_D is negative and V_G is swiped from +5V to -5V for (a) $V_{backgate}$ = 0V, (b) $V_{backgate}$ = +4V (c) $V_{backgate}$ = -4V.

Figure 3.4(a to c) shows the I_D-V_D characteristics, when V_D is negative and for different values of $V_{backgate}$. It is found that transistor output characteristics exhibit saturation and hence for negative V_D application p-type Si-NW shows perfect transistor behavior. Application of back gate voltages also found to change drive current level. For $V_{backgate}$=4V, I_D values are found to be lowest for same bias conditions among the three conditions simulated. At $V_{backgate}$=+4V significant depletion of p-type NW is expected and hence, I_D values becomes lower than that of the $V_{backgate}$=0V where as for $V_{backgate}$=-4V, I_D value is high as carrier accumulator occurs at this condition.

Figure 3.5(a to c) shows sensitivity as a function of gate voltages for different values of positive V_D applications. The results are presented for different backgate bias conditions. For $V_{backgate}$=0V, the maximum sensitivity is 2.0×10^4%/V at V_G=0V which reduces to value of 6.45 %/V at V_G=-5V for V_D=0.5V. The sensitivity was calculated using first order equation $[(I_2-I_1) \times 100] / [I_2 (-V_{G2}+V_{G1})]$ to show % change in conductance's when biomarkers will be attached on the top gate. For V_D=1V sensitivity for any fixed V_G is lower than V_D=0.5V. However, good sensitivity can still be ensured by setting a required V_G values at the top gate using liquid gating. For example a sensitivity of 1.92×10^3%/V can be set with V_G=0V at V_D=1V condition. Further increase of V_D values found to shift the sensitivity curve to more positive V_G values thereby reducing sensitivity for any found V_G application. This shift can be explained by the presence of huge DIBL in the sub-threshold characteristics for positive V_D application as shown in figure 3.1(a).These results are very important for ensuring maximum sensitivity operation of p-type Si-NW biosensor where NW dimensions are 100nm thick and 1µm long with a body doping of 10^{16}/cm^3. For example V_D=0.5V has a sensitivity of 1.93×10^3%/V can be set without any liquid gating. However, this level of conductance change may not be at all detectable by conventional B1500 semiconductor parameter analyzer as this point corresponds to a current level of 10^{-15}A/µm which may not at all be detected. For V_D=1V when V_G=0 sensitivity is 1.92×10^3%/V, which is actually quite good. Figure 3.1(a) shows that current level at this condition is around 10^{-7}A/µm which is actually excellent for detection. To achieve sensitivity greater than 1.92×10^3%/V without any liquid gating while maintaining good detection capacity with conventional parameter analyzer may be a current level of 10^{-9}A/µm(fig 3.1a) which would required a $V_D \approx 0.9$V as can be seen from figure 3.1a and figure 3.6a respectively. As such, these results provides crucial information for bias set up in p-type Si-NW based biosensors for ensuring molecular level detection. On one side required bias point can be pre determined when no liquid gating would be provided. On the other side, if costly liquid gating can be arranged V_D can be set to any level while required V_G values for liquid gate can be pre determined for p-type NWs from these analyses. For example if V_D=2V, NW will exhibit a sensitivity of 4.85×10^2%/V when no liquid gating is provided. However, if a liquid gating of V_G=0.5Vis provided it will exhibit a sensitivity of 1.93×10^3%/V.
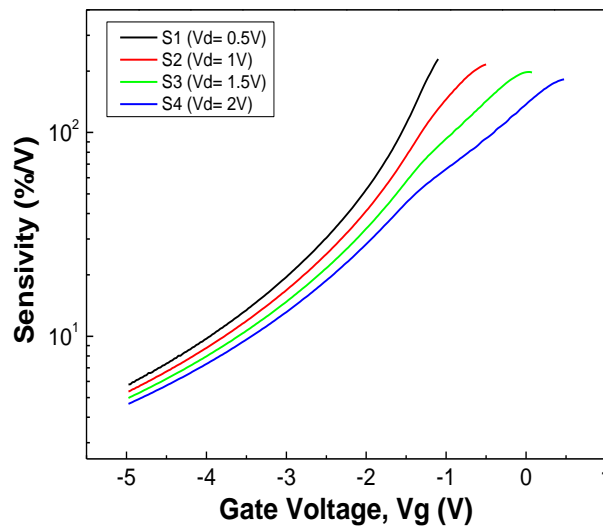
Figure 3.5 Shows sensitivity characteristics (Sensitivity vs V_G) of Si-NW when V_D is positive and V_G is swiped from +5V to -5V for (a) $V_{backgate} = 0V$, (b) $V_{backgate} = +4V$ (c) $V_{backgate} = -4V$.

Figure 3.5(b) shows sensitivity as a function of gate voltages for different values of positive V_D applications when backgate bias has been set to +4V. In general, sensitivity is almost similar to the case when $V_{backgate}$ was set to 0V. This result imply that carrier depletion beyond $10^{16}/cm^3$ does not significantly change sensitivity of p-type Si-NW of 1μm long and 100nm thickness.

Figure 3.5(c) shows sensitivity as a function of gate voltages for different values of positive V_D applications when backgate bias has been set to -4V. For $V_{backgate}$ of -4V degradation of sensitivity can be observed implying that significant carrier accumulator or heavy doping in NWs would reduce its sensitivity as biosensor. However, figure 3.5(a to c) shows an excellent way to tailor NW biosensor sensitivity in SOI platform via backgate arrangement.
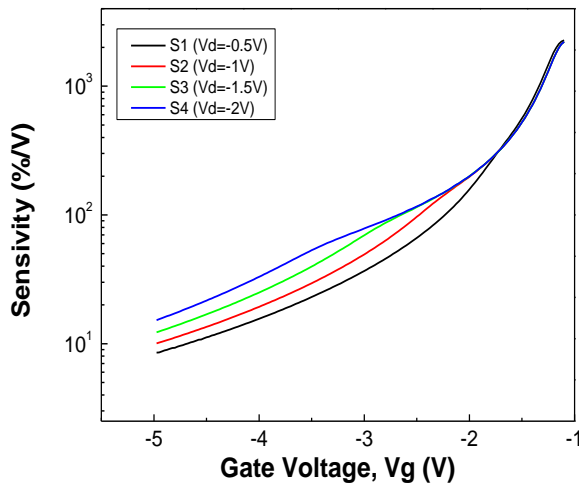
(a)
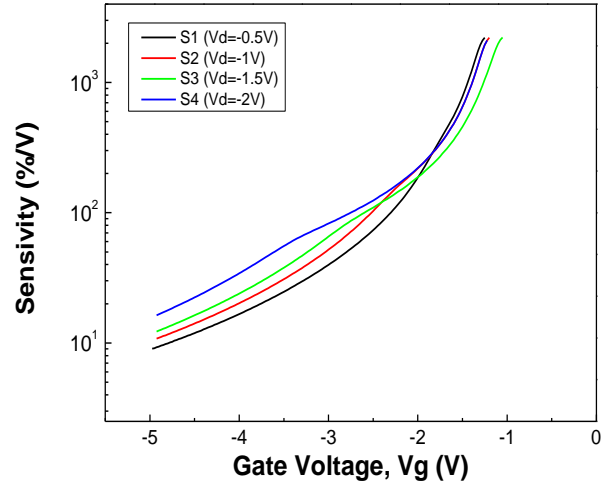
(b)
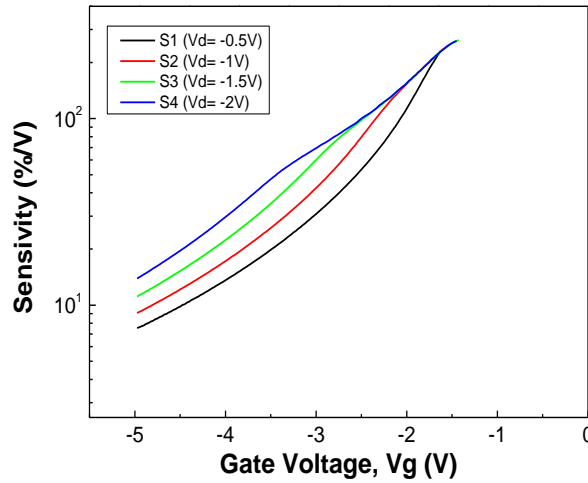
(c)

Figure 3.6 Shows sensitivity characteristics (Sensitivity vs V_G) of Si-NW when V_D is negative and V_G is swiped from +5V to -5V for (a) $V_{backgate} = 0V$, (b) $V_{backgate} = +4V$ (c) $V_{backgate} = -4V$.

Figure 3.6(a to c) show sensitivity as a function of top gate voltages where V_D is negative. Results are presented for different values of backgate bias. For $V_{backgate}$=0V in figure 3.6(a) it is observed that sensitivity at V_G=-1V is 2.27×10^3 %/V which reduces to a value of 8.53 %/V at V_G=-5V. As discussed before, a accurate level of $1e^{-9}$ A/µm can be set as a reasonable current which requires a top gate voltage of -1V while V_D=0.5V. At this condition achievable sensitivity is 2.27×10^3%/V. In contrast to positive V_D application (fig. 3.5) there is no significant shift ofsensitivity curves at higher negative V_D values (fig. 3.6) which can be explained by ideal sub-threshold characteristics of figure 3.2 with no DIBL. However, absence of DIBL for negative V_D applications is somehow not beneficiary for sensing operation as it mandates liquid gating of the top gate to set required V_G values for sensitive operation. For example V_D=-0.5V, a V_G=-1V is required to set detectable level of current at the same time to achieve maximum sensitivity. It is also worth nothing that with increasing negative V_D values sensitivity does not change too much which is not similar to the behavior observed when V_D was positive. An almost similar characteristic can be observed in figure 3.6(b) for $V_{backgate}$=+4V with significant depletion of NW. However, sensitivity significantly decreases for $V_{backgate}$=-4V when carrier accumulator is done by back gate. It is worth noting that all characteristics with negative V_D is confined in negative V_G region thereby mandatory liquid gating sensitive operation as biosensor.

CHAPTER 4: DISCUSSION

The investigation reveals that Si-NW sensitivity depends significantly on backgate bias and also on the polarity of drain voltages. The dependence on the polarity of drain voltages can be explained by depletion region on the drain side. When positive drain voltage is applied p^+p junction is actually forward biased and hence, there should be a noticeable effect of drain voltages on the source-body potential barrier as can be seen by the presence of DIBL on the sub-threshold characteristics of p-type Si-NW when V_D is positive. Such a DIBL has actually beneficiary effect as it allowed getting maximum sensitive operation without any liquid gating of top gate. When V_D is negative p^+p junction is reverse biased and hence, there should be less effect of drain voltage on source-body potential barrier as can be seen from less DIBL in the sub-threshold characteristics when V_D is negative. As discussed before such a characteristics mandates requirement of liquid gating for maximum sensitive operation of p-type Si-NW as biosensor. Being p-type NW positive backgate voltage significantly depletes NW body thereby making it more sensitive to top gate voltages. When negative back gate voltage is applied carriers accumulator occur which makes Si-NW less sensitive top gate voltages and hence, explains the sensitivity tuning using backgate.

CHAPTER 5: CONCLUSION

We have performed a feasibility study of tailoring sensitivity of Si nanowire through backgate bias arrangement for Biosensing application. A 100nm thick and 1µm nanowire with doping concentration of 10^{16} cm^{-3} is investigated for different backgate voltages. We have found that backgate bias has significant effect on the sensitivity of p-type Si-NW. Backgate bias for depletion of NW body is found to increase sensitivity of NWs whereas backgate bias for significant carrier accumulation is found to decreases sensitivity of NW. Sensitivity trend of NWs also found to depend on the polarity of drain voltages. When drain voltage is positive, presence of DIBL on the sub-threshold characteristics is found to exhibit sensitivity curve towards positive top gate voltage with increasing drain voltages. Presence of DIBL on sub-threshold characteristics is somehow found to beneficiary for biosensing application as it provides maximum sensitive operation of Si-NW even without any liquid gating of the top gate. Considering current detection capacities of semiconductor parameter analyzer available in the market at positive drain voltage of 0.9V is found to provide a maximum sensitivity of 2×10^{3}%/V even without any liquid gating. Simulation also shows that it is possible to get NWs sensitivity greater than 2×10^{3}%/V using liquid gating and providing drain voltages less than 0.5V. When drain voltage is negative no DIBL is observed in the sub-threshold characteristic which mandates liquid gating of the top gate for maximum sensitive operation of Si-NW as biosensor. These results are very significant of p-type Si-NW based biosensors fabricated on SOI platform to ensure maximum sensitive operation for molecular level detection.

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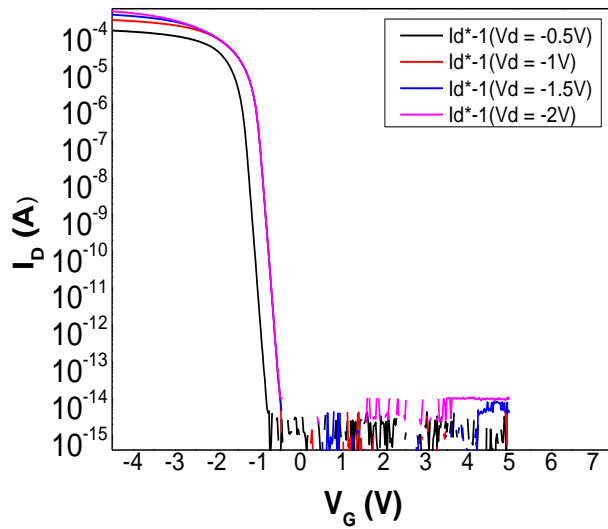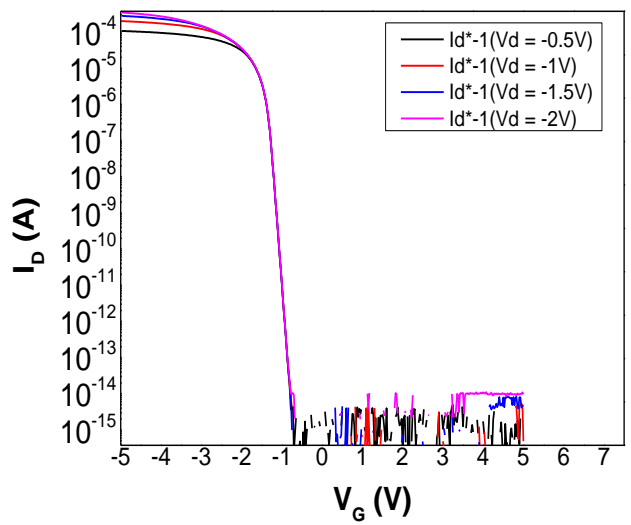
Fig 1: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate} = 0V$ when V_D positive
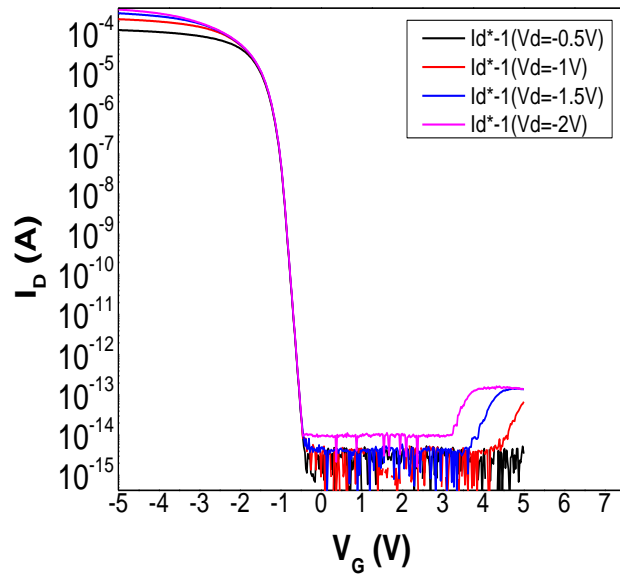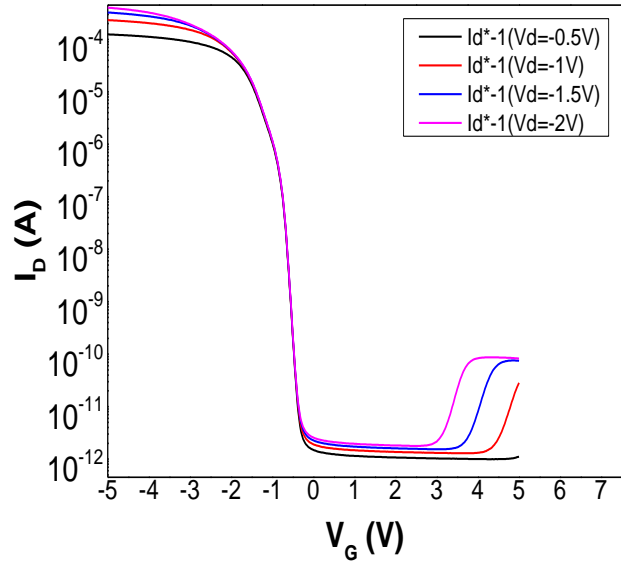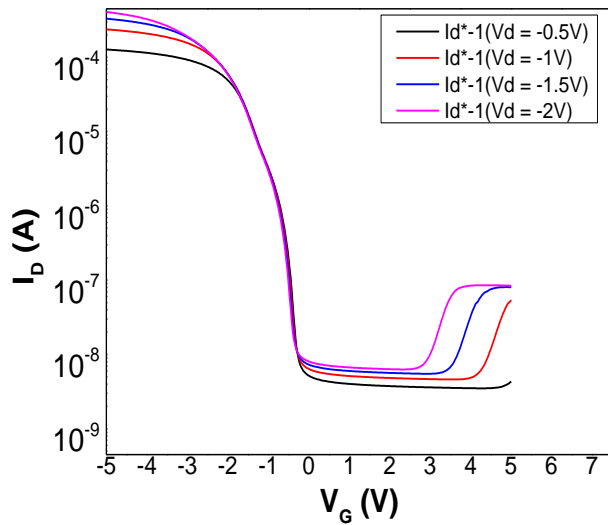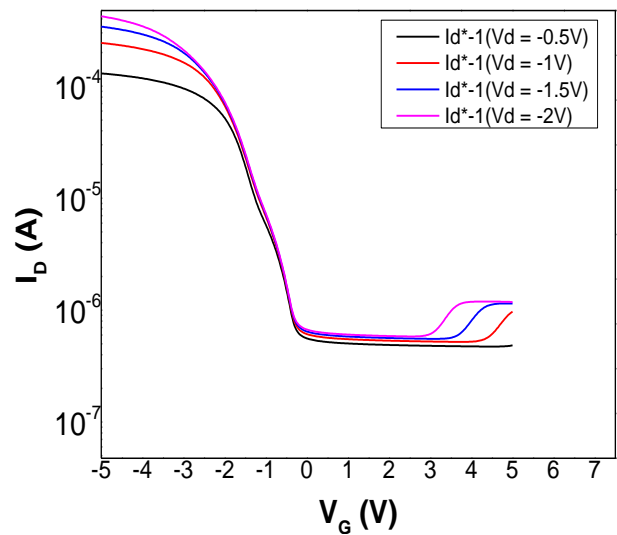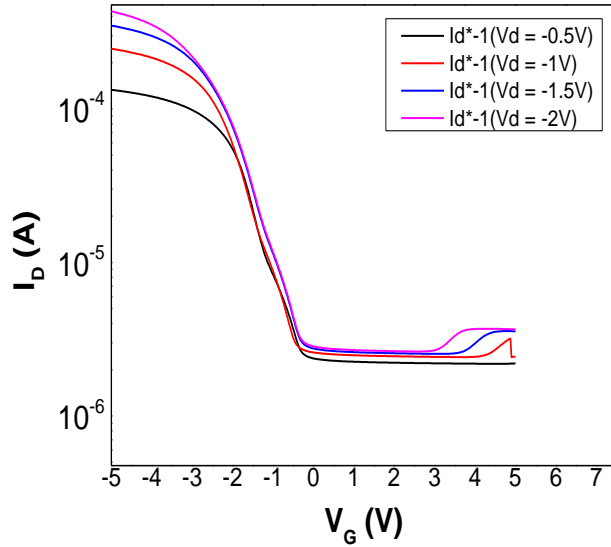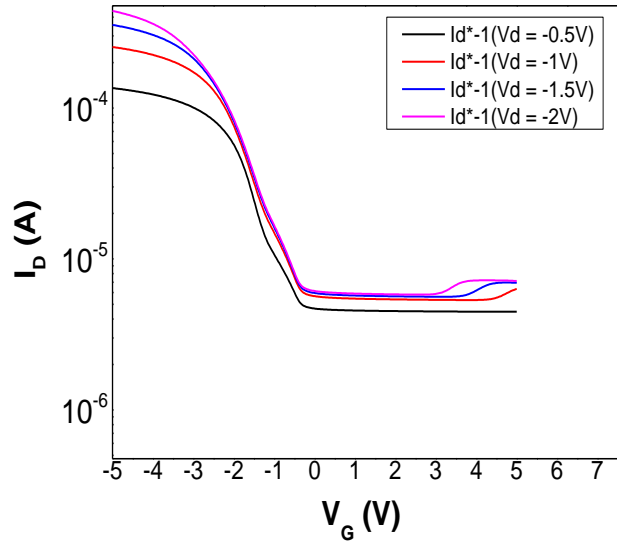

Fig 2: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate} = 1V$ when V_D positive

Fig 3: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate} = 2V$ when V_D positive

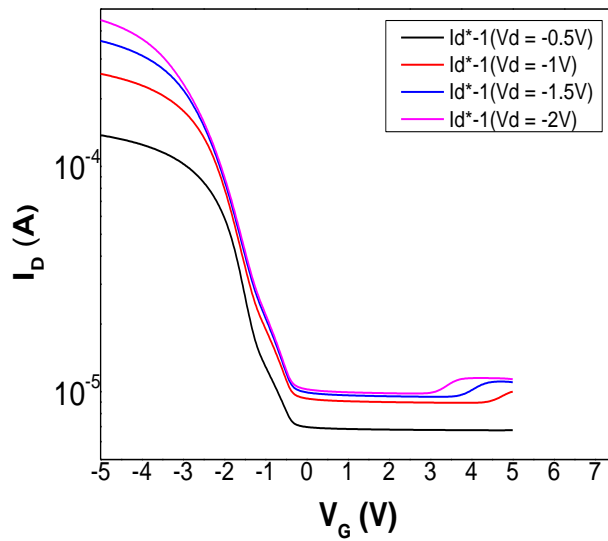**Fig 4:** Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate} = 3V$ when V_D positive

Fig 5: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate} = 4V$ when V_D positive

Fig 6: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate} = 5V$ when V_D positive

Fig 7: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate} = 6V$ when V_D positive

Fig 8: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate} = 7V$ when V_D positive

Fig 9: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = -1V when V_D positive

Fig 10: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = -2V when V_D positive

Fig 11: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = -3V when V_D positive

Fig 12: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = -4V when V_D positive

Fig 13: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = -5V when V_D positive

Fig 14: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = -6V when V_D positive

Fig 15: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = -7V when V_D positive

APPENDIX A₂

Fig 1: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for V_Backgate = 0V when V_D negative

Fig 2: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for V_Backgate = 1V when V_D negative

Fig 3: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for V_Backgate = 2V when V_D negative

Fig 4: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for V_Backgate = 3V when V_D negative

Fig 5: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = 4V when V_D negative

Fig 6: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = 5V when V_D negative

Fig 7: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = 6V when V_D negative

Fig 8: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = 7V when V_D negative

Fig 9: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = -1V when V_D negative

Fig 10: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = -2V when V_D negative

Fig 11: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = -3V when V_D negative

Fig 12: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = -4V when V_D negative

Fig 13: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = -5V when V_D negative

Fig 14: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = -6V when V_D negative

Fig 15: Simulated transfer characteristics (I_D vs V_G) of Si-NWs for $V_{Backgate}$ = -7V when V_D negative
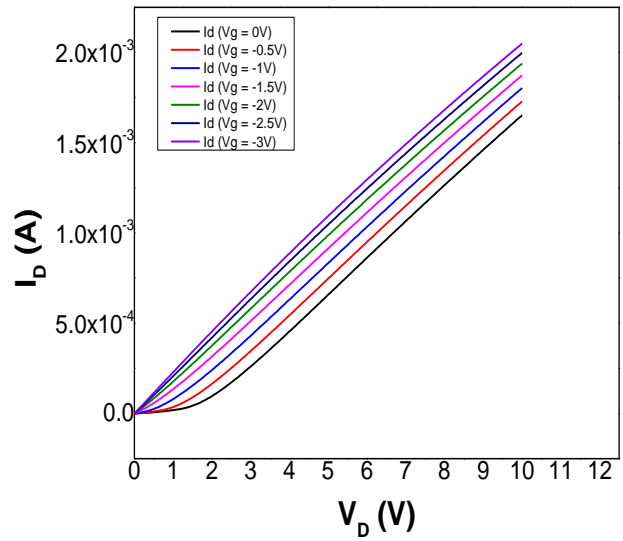
Fig. 1: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate} = 0V$ when V_D positive

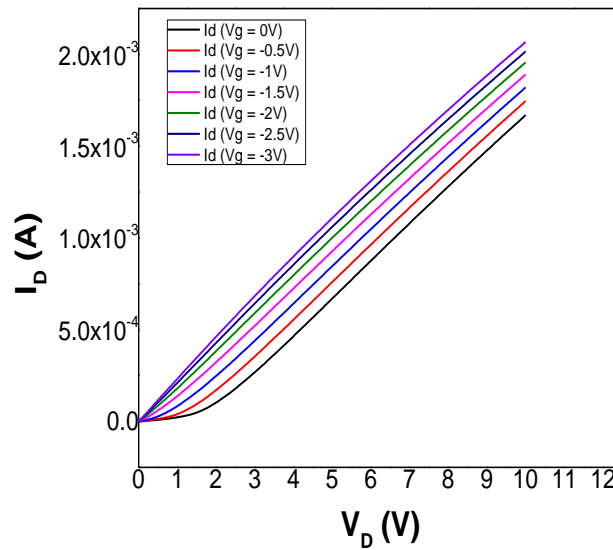**Fig. 2:** Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate} = 1V$ when V_D positive
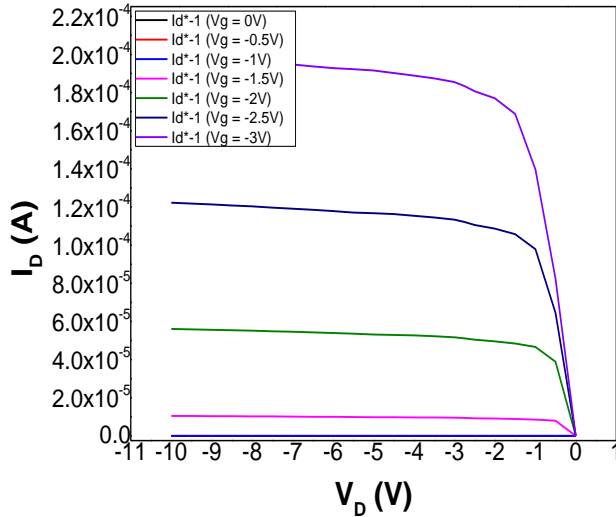

Fig. 3: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate} = 2V$ when V_D positive

Fig. 4: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate} = 3V$ when V_D positive

Fig. 5: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = 4V when V_D positive
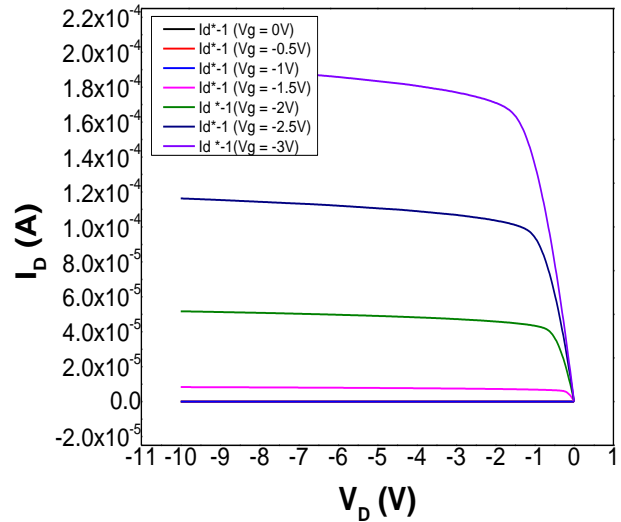

Fig. 6: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = 5V when V_D positive
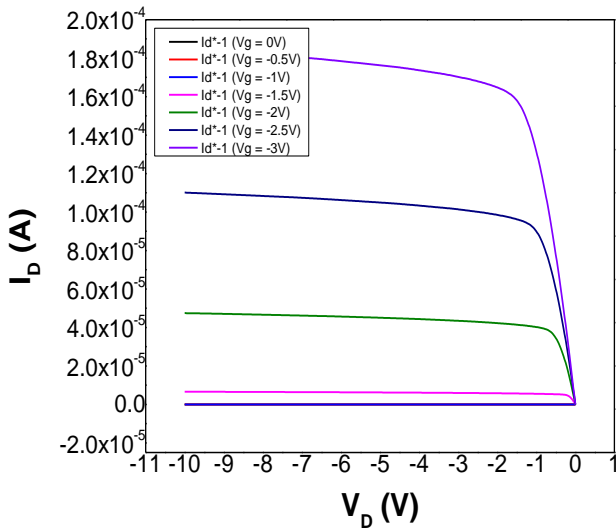

Fig. 7: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = 6V when V_D positive
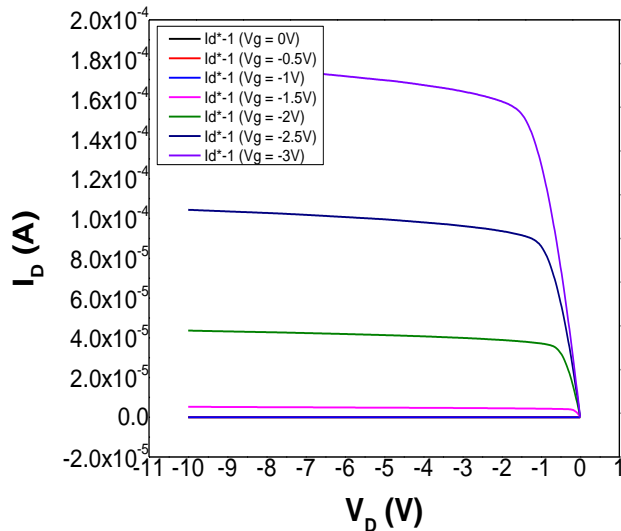

Fig. 8: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = 7V when V_D positive

Fig. 9: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = -1V when V_D positive
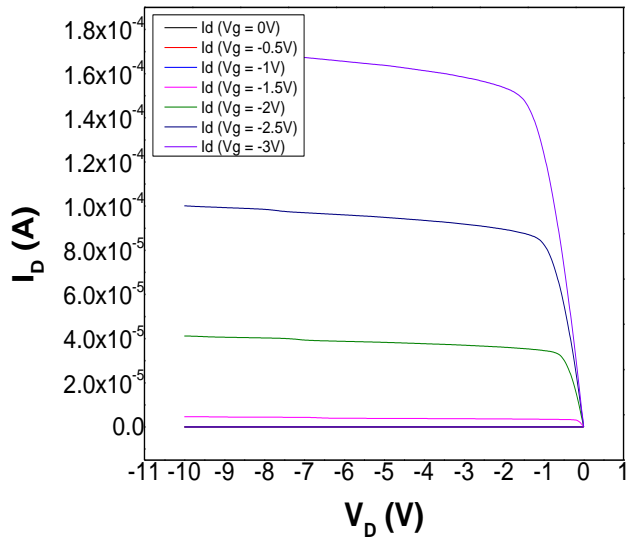

Fig. 10: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = -2V when V_D positive

Fig. 11: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = -3V when V_D positive

Fig. 12: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = -4V when V_D positive
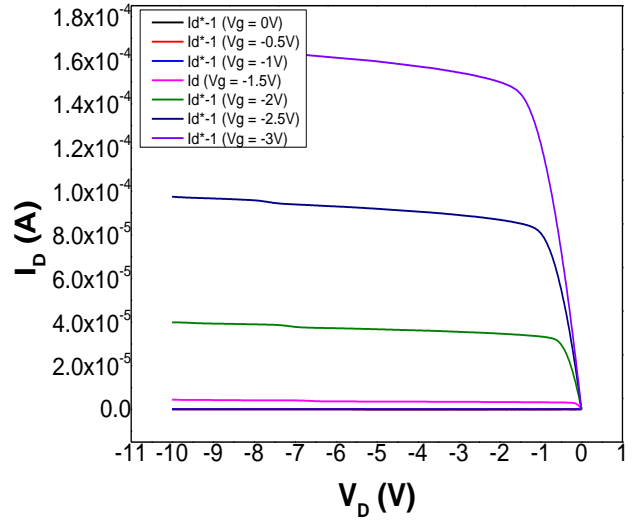
Fig. 13: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = -5V when V_D positive
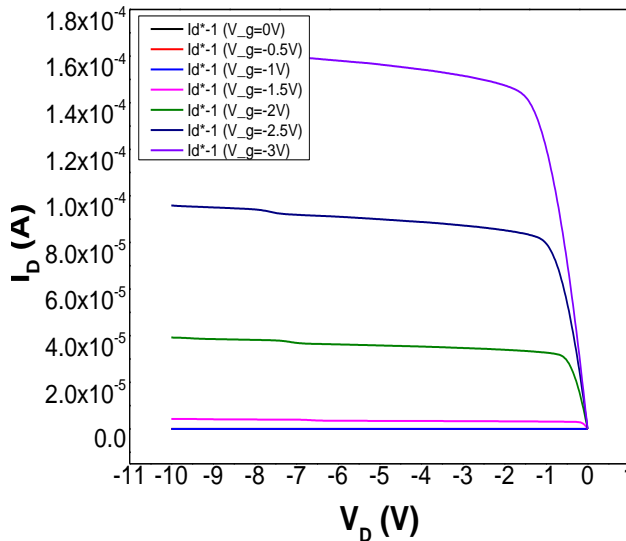
Fig. 14: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = -6V when V_D positive

Fig. 15: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = -7V when V_D positive
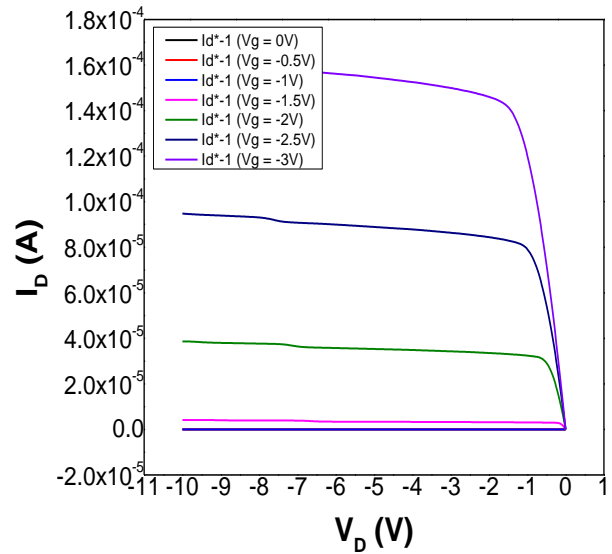
Fig. 1: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate} = 0V$ when V_D negative

Fig. 2: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate} = 1V$ when V_D negative

Fig. 3: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate} = 2V$ when V_D negative

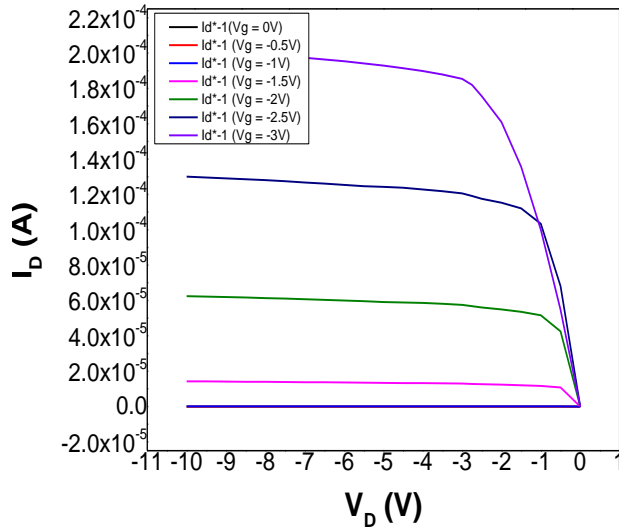**Fig. 4:** Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate} = 3V$ when V_D negative
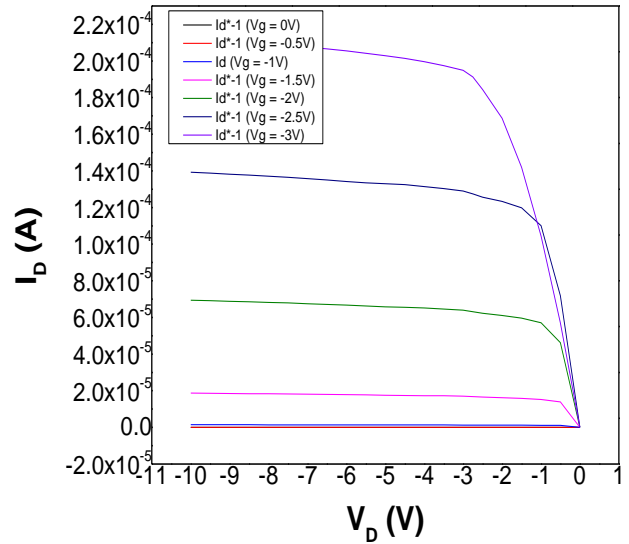
Fig. 5: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = 4V when V_D negative
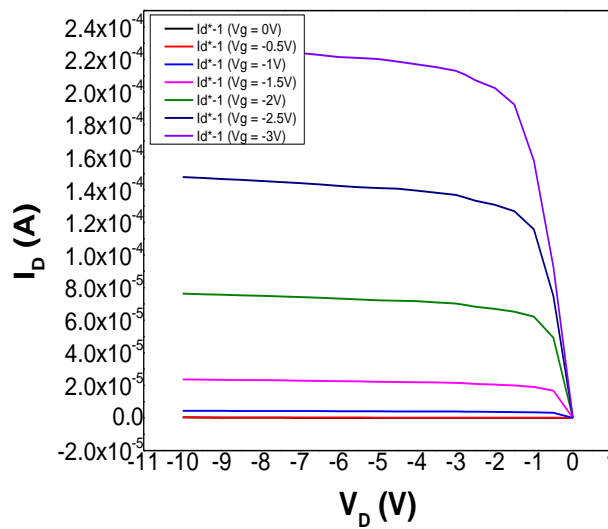

Fig. 6: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = 5V when V_D negative

Fig. 7: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = 6V when V_D negative

Fig. 8: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = 7V when V_D negative

Fig. 9: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = -1V when V_D negative
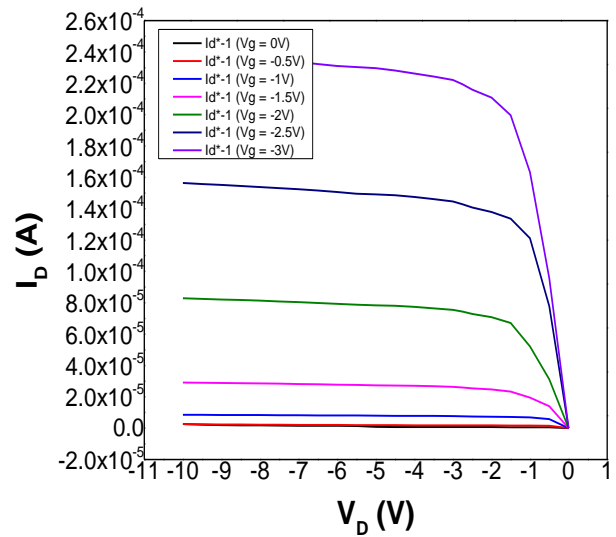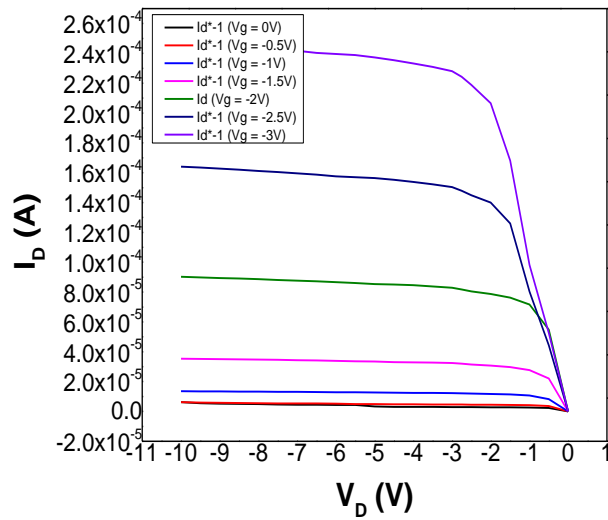

Fig. 10: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = -2V when V_D negative

Fig. 11: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = -3V when V_D negative

Fig. 12: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = -4V when V_D negative

Fig. 13: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = -5V when V_D negative
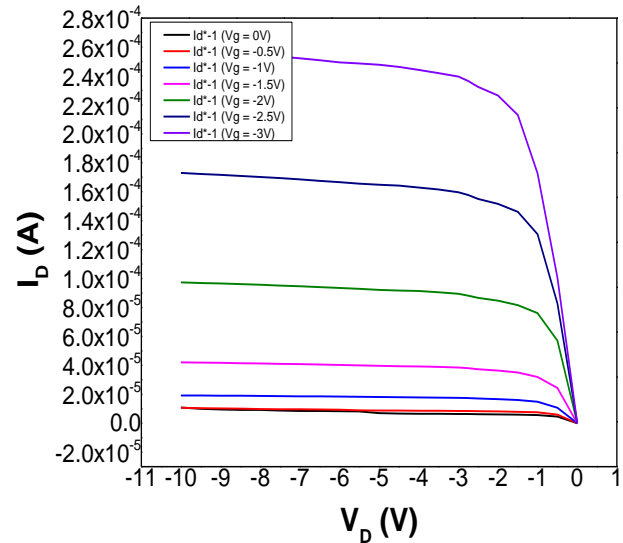

Fig. 14: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = -6V when V_D negative
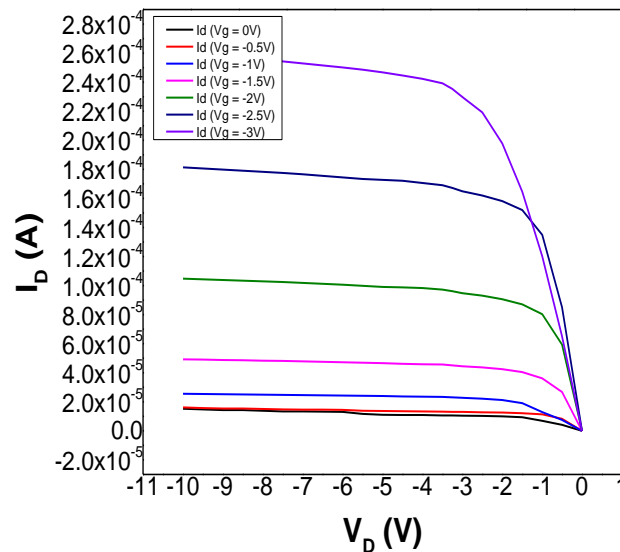

Fig. 15: Simulated output characteristics (I_D vs V_D) of Si-NWs for $V_{Backgate}$ = -7V when V_D negative